A Positive Output Buck-Boost Converter with Extensive Linear Conversion Ratio Adjustment Range

Nguyen Van Ban
Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam
banvn.ncs@hcmute.edu.vn

Pham Vo Hong Nghi
Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam
nghi.pvh.cv@gmail.com

Quach Thanh Hai
Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam
haiqt@hcmute.edu.vn

Truong Viet Anh
Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Vietnam
anhtv@hcmute.edu.vn (corresponding author)

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ABSTRACT

The article introduces a non-isolated positive output buck-boost converter that is capable of operating across a wide duty cycle range. The converter exhibits low nonlinearity in its voltage gain relative to *D*, thereby enhancing its capability to regulate output voltage or effectively regulate current over a broad duty cycle spectrum. A comparison of the performance of the proposed converter with existing converters is presented, with a particular consideration of the DC gain, voltage and current stresses on switches and diodes, and inductor currents. The comprehensive calculations include ideal and practical voltage gains, current assessments, stress analysis on components, parameter design, efficiency, and brief discussions on the discontinuous conduction mode and boundary conditions. The converter exhibits peak efficiencies of approximately 98.98% in boost mode and 99.16% in buck mode, which represent a notable advancement in power electronics. It is noteworthy that the converter displays minimal current and voltage overshoot in buck mode with a conversion ratio below 3. The overshoot relative to the normalized current is less than 1, reaching a minimum of 0.21, while the voltage overshoot is as low as 0.51. This contributes to superior buck mode efficiency. A laboratory model was developed with great care to validate the converter's experimental outcomes and theoretical evaluations. This provides reassurance about the reliability of the research.

Keywords-buck-boost; non-isolated; positive output; dc-dc converter; voltage gain

I. INTRODUCTION

The functionality of renewable energy systems, which encompass photovoltaic panels, backup power supplies, mobile devices, industrial equipment, and telecommunications systems, hinges upon the availability of stable power supplies that adhere to stringent voltage regulations. This highlights the vital function of DC-DC converters in renewable energy systems, which are essential for attaining the requisite voltage levels [1, 2]. The output voltage from renewable sources may be low, high, or variable, necessitating stabilization. It is therefore evident that the work of engineers and researchers in

developing and enhancing DC-DC converters, such as boost, buck, and buck-boost converters, is of significant importance. Their contribution is of great consequence in addressing the challenges posed by fluctuating output voltage and in advancing the field [3].

A boost converter is capable of increasing the input voltage, whereas a buck converter is limited to lowering the input voltage. The buck-boost converter, which is capable of increasing and decreasing the input voltage, offers a flexible solution [4]. Due to its distinctive features, it is beneficial for a variety of applications, including LED drivers, battery chargers, portable electronic devices, wind energy production, telecommunications, and more. Its versatility renders it a valuable instrument in the renewable energy industry [5-7]. The DC-DC buck-boost converter is not only a vital component, but also a fundamental element that is critical to the success of the Maximum Power Point Tracking (MPPT) process. The converter plays a pivotal role in enhancing energy efficiency by meticulously regulating the voltage and current from the solar panel, even when confronted with considerable fluctuations in environmental conditions and load. The converter's flexibility and optimization capabilities ensure that the system consistently operates at the maximum power point, thereby making it indispensable for achieving the highest efficiency and maintaining long-term stability in solar energy systems. The three types of DC-DC converters [5–7], are classified as non-isolated converters. Non-isolated converters are employed more frequently than their isolated counterparts due to their high efficiency, compact size, low cost, and minimal input current ripple [8-10]. Such converters are typically employed in low-power applications due to their uncomplicated design, high efficiency, and cost-effective implementation [11]. In the case of buck-boost converters using the two proposed switches [12-19], it is observed that although they offer high voltage gain they have a narrow controllable duty cycle range (D). The ratio of V_o/V_i concerning D across the entire range includes segments with steep slopes, as shown in Figure 1, and significant nonlinearity (when $D >$ 0.65), which results in a discrepancy between the actual voltage boost and the expected results predicted by the voltage amplification relation when the input voltage conditions change [20]. In renewable energy systems, such as solar power systems, high voltage gain is unnecessary since the input voltage from the solar panels is typically in close proximity to the load's required voltage. Minor adjustments to the DC-DC buck-boost converter are sufficient to maintain optimal voltage, thereby maximizing efficiency and reducing energy loss. As presented in Figure 1, a converter with a linear voltage conversion ratio based on the duty cycle can regulate the operating point from a specific position, such as point M to point N, with a sufficiently broad ΔD_3. In contrast, the control of converters [12-19] is more challenging due to the narrow control regions, ΔD_1 and ΔD_2, that they exhibit. This has an impact on the accuracy of the output voltage. In order to achieve a more precise output voltage, further Pulse Width Modulation (PWM) is required. Nevertheless, reducing the width of the PWM pulses remains a significant challenge, as it depends on the resolution of the microcontroller's timers, clock pulse frequency, and especially the stability of the power supply. This study introduces a practical buck-boost DC-DC structure that employs two switches, two diodes, two inductors, and two capacitors. The structure is designed to provide buck-boost functionality with an appropriate voltage gain ratio and a wide duty cycle range (experimentally achieved D = 0.1 ÷ 0.8). In buck mode, the output voltage to input voltage ratio is nearly linear with the duty cycle. In boost mode, the structure exhibits low nonlinearity across the entire range (0.38 ÷ 0.8), enabling better output voltage control.

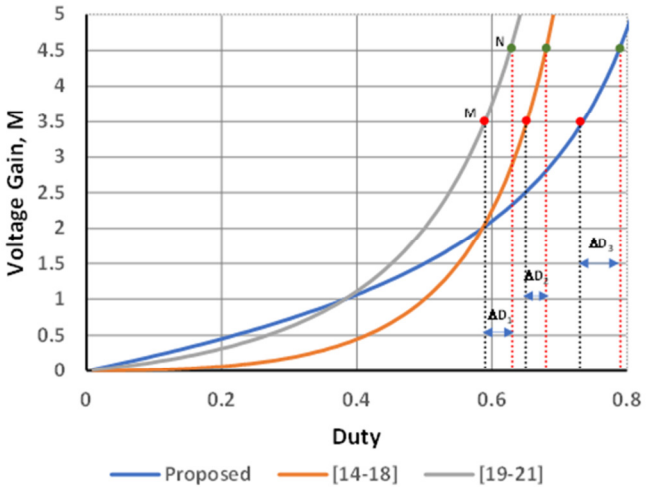

Fig. 1. A comparison of ideal voltage gain against duty cycle.

The experimental results of the prototype validated the evaluations, analyses, and comparisons. The output voltage parameters met the specified requirements and aligned with the theoretical calculations, thereby validating the design. The key highlights of the proposal are reflected in the following recommendations:

- The converter is capable of providing voltage boosting and reducing capabilities with a positive output voltage.
- The converter offers a wide duty cycle range (0 < D < 0.8) with a broad linear control region, rendering it suitable for applications that necessitate a stable power supply and precise voltage control.
- The device features a continuous current waveform and a shared ground for the input and output.
- The analyses and assessments demonstrated that the efficiency was higher with lower current and voltage stress parameters than those observed in previous studies [12-19].

II. PROPOSED CIRCUIT STRUCTURE

The converter presented in Figure 2 has been optimized for stability. The former includes a pair of switches, each equipped with two inductors (L_1 and L_2), two capacitors (C_1 and C_0), and a pair of diodes ($D1$ and $D2$). The converter's operation is portrayed in Figure 3, which presents various time-domain waveforms. The high-frequency operation, which is managed by two switches (S_1 and S_2) operating at 40 kHz, effectively reduces the size of the inductors and minimizes power losses,

including both core and copper losses. The switches are synchronized, enabling two distinct operating modes. The selected inductors and capacitors are of a sufficient size to maintain Continuous Conduction Mode (CCM) and ensure consistent voltage stability, thereby providing reliable performance. Further details regarding the operational modes are provided in Sections A and B.

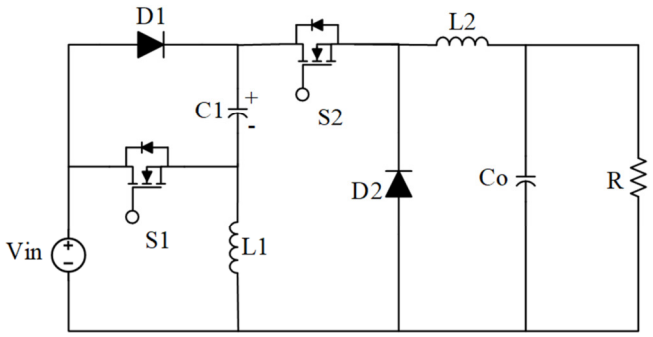

Fig. 2. A schematic diagram of the proposed converter.

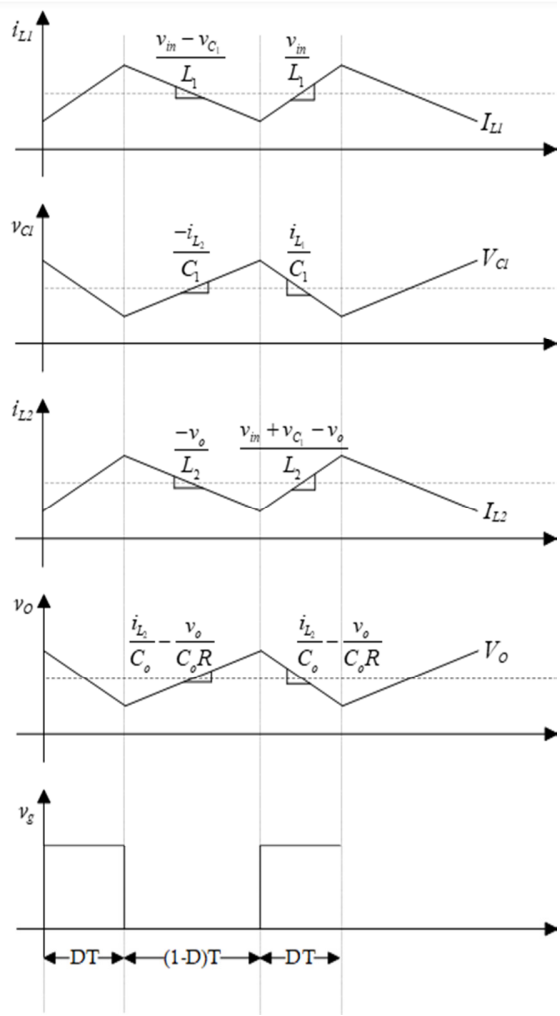

Fig. 3. Various time-domain waveforms of the proposed converter.

A. Initial Phase

The power switches S_1 and S_2 are activated for a duration determined by a duty cycle DT, as depicted in Figure 4. During this period, diodes D_1 and D_2 remain reverse-biased. During this interval, the input voltage V_{in} provides energy to the inductor L_1, while simultaneously, the capacitor C_1 and the aforementioned voltage source supply energy to the inductor L_2. The voltage across capacitor C_1 serves as a reflection of the voltage stress on diode D_1 and switch S_1, which is of paramount importance for the evaluation of the circuit's performance and the identification of potential issues. The governing differential formulas are detailed in (1).

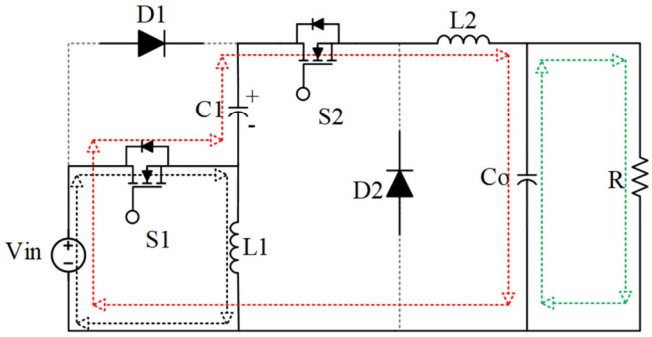

Fig. 4. Initial phase.

$$\begin{cases} L_1 \frac{\mathrm{di}_{L_1}}{\mathrm{dt}} = \mathrm{v_{in}} \\ L_2 \frac{\mathrm{di}_{L_2}}{\mathrm{dt}} = \mathrm{v_{in}} + \mathrm{v}_{C_1} - \mathrm{v}_o \\ C_1 \frac{\mathrm{dv}_{C_1}}{\mathrm{dt}} = -\mathrm{i}_{L_2} \\ C_o \frac{\mathrm{dv}_o}{\mathrm{dt}} = \mathrm{i}_{L_2} - \frac{v_o}{R} \end{cases} \quad (1)$$

B. Second Phase

As can be seen in Figure 5, switches S_1 and S_2 are turned off for the interval $(1-D)T$ during which diodes D_1 and D_2 are in forward bias.

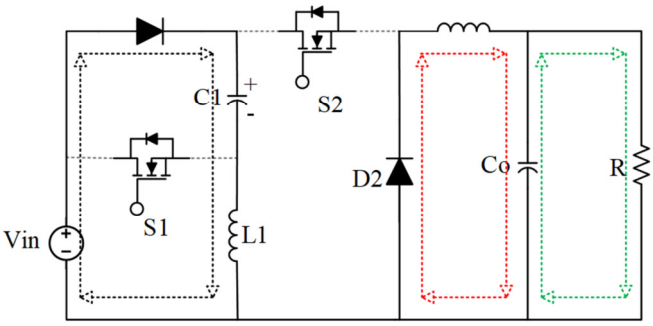

Fig. 5. Second phase.

$$\begin{cases} L_1 \frac{\mathrm{di}_{L_1}}{\mathrm{dt}} = \mathrm{v}_{\mathrm{in}} - v_{C_1} \\ L_2 \frac{\mathrm{di}_{L_2}}{\mathrm{dt}} = -\mathrm{v}_o \\ C_1 \frac{\mathrm{dv}_{C_1}}{\mathrm{dt}} = \mathrm{i}_{L_1} \\ C_o \frac{\mathrm{dv}_o}{\mathrm{dt}} = \mathrm{i}_{L_2} - \frac{v_o}{R} \end{cases} \quad (2)$$

The input voltage V_{in} charges capacitor C_1 via diode D_1. Simultaneously, inductor L_2 supplies energy to the output capacitor C_o through diode D_2. The voltage stress on switch S_1 corresponds to the voltage across capacitor C_1, while the stress on switch S_2 equals V_{in}. The associated differential formulas are derived as detailed in (2).

C. Voltage Conversion Ratio

In steady-state operation, the inductors function as short circuits, resulting in an average voltage over a zero-duty cycle. Applying the principle of volt-second balance to (1) and (2) leads to the derivation of (3):

$$\begin{cases} DV_{in} + (1-D)\left(V_{in} - V_{C_1}\right) = 0 \\ D\left(V_{in} + V_{C_1} - V_o\right) + (1-D)(-V_o) = 0 \end{cases} \quad (3)$$

The voltages across capacitors C_1 and C_o are determined respectively by (4) and (5), derived from (3):

$$V_{C_1} = \frac{V_{in}}{1-D} \quad (4)$$

$$V_o = \frac{V_{in}(2D-D^2)}{1-D} \quad (5)$$

Accordingly, the voltage conversion ratio (M) of the proposed converter can be calculated in compliance with the description provided in:

$$M = \frac{V_o}{V_{in}} = \frac{2D-D^2}{1-D} \quad (6)$$

D. Charge-Second Balance

Applying the Charge-second balance law to (1) and (2) in the two operating stages of the circuit, the current through the inductors is determined by (7), where $I_o = V_o/R$:

$$I_{L_1} = \frac{D}{1-D} I_o, I_{L_2} = I_o \quad (7)$$

E. Voltage and Current Stress Analysis

The voltage stress on the diodes and power switches is the maximum voltage applied to them during operation and can be determined by:

$$V_{S_1} = V_{D_1} = \frac{V_{in}}{1-D} \quad (8)$$

$$V_{D_2} = \frac{(2-D)V_{in}}{1-D} \quad (9)$$

$$V_{S_2} = V_{in} \quad (10)$$

Based on the operating principle, the current flowing through switch S_1 can be calculated using:

$$i_{S_1}(t) = \begin{cases} i_{L_1}(t) + i_{L_2}(t) & (0, DT) \\ 0 & (DT, T) \end{cases} \quad (11)$$

From (11), the average current through the power switch S_1 can be determined, as:

$$I_{S_1} = \frac{D}{1-D} I_o \quad (12)$$

The current through diode D_1 can be determined by (13), and the average current through the diode is determined following (14):

$$i_{D_1}(t) = \begin{cases} 0 & (0, DT) \\ i_{L_1}(t) & (DT, T) \end{cases} \quad (13)$$

$$I_{D_1} = DI_o \quad (14)$$

Based on the operating principle, the current through switch S_2 can be calculated using:

$$i_{S_2}(t) = \begin{cases} i_{L_2}(t) & (0, DT) \\ 0 & (DT, T) \end{cases} \quad (15)$$

Based on (15), the average current flowing through the power switch S_2 is calculated as indicated in:

$$I_{S_2} = DI_o \quad (16)$$

The current through diode D_2 can be determined by (17), and the average current through the diode is determined following (18):

$$i_{D_2}(t) = \begin{cases} 0 & (0, DT) \\ i_{L_2}(t) & (DT, T) \end{cases} \quad (17)$$

$$I_{D_2} = (1-D)I_o \quad (18)$$

F. Evaluation of Voltage and Current Ripple

$$\begin{cases} \Delta i_{L_1} = \frac{DV_{in}}{f_S L_1} \\ \Delta i_{L_2} = \frac{(2-D)DV_{in}}{f_S L_2} \\ \Delta v_{C_1} = \frac{D^2 I_o}{(1-D) f_S C_1} \\ \Delta v_{C_o} = \frac{(2-D)DV_{in}}{8 f_S^2 L_2 C_o} \end{cases} \quad (19)$$

Equation (19) provides the current waveform through the inductor and the voltage waveform across the capacitor. These characteristics are crucial for selecting the appropriate components, with f_s indicating the switching frequency of the power switch.

G. Boundary between Continuous Conduction Mode and Discontinuous Conduction Mode

The shift from CCM to DCM is signified by $I_{L_1} = \Delta i_{L_1}/2$ and $I_{L_2} = \Delta i_{L_2}/2$. These values are crucial for determining the transition, as they signify the inductor current reaching its minimum of zero. To verify if the proposed converter operates in CCM, (7) and (19) should be used to input values into the condition outlined in (20), where R denotes the load resistance:

$$\begin{cases} L_1 > \frac{(1-D)^2 R}{(4D-2D^2) f_s} \\ L_2 > \frac{(1-D)R}{2 f_s} \end{cases} \quad (20)$$

H. Power Loss Analysis

The total power loss in the inductor includes copper losses due to winding resistance r_L and core losses from hysteresis and eddy currents in the magnetic core. Using (7), the approximate RMS value of the current through the inductors can be determined by:

$$I_{L_{1}(RMS)} = \sqrt{\frac{1}{T}\int_0^T i_{L_1}^2(t)\,dt} \approx \frac{D}{1-D} I_o \quad (21)$$

$$I_{L_{2}(RMS)} = \sqrt{\frac{1}{T}\int_0^T i_{L_2}^2(t)\,dt} \approx I_o \quad (22)$$

Copper loss in the inductor can be calculated from (21) and (22) and is determined by (23):

$$P_{L_C} = I_{L_1(RMS)}^2 r_{L_1} + I_{L_2(RMS)}^2 r_{L_2} = \left(\frac{D^2 r_{L_1}}{(1-D)^2} + r_{L_2}\right)\frac{P_o}{R} \quad (23)$$

where, the output power P_o is determined by multiplying V_o with I_o. The core loss density for the inductor can be approximated using the revised loss formula, which is derived from the core material's characteristic curve as described in:

$$\Delta P_{L\_Co} = aB^b f^c \quad (24)$$

In this context, a, b, and c are determined by fitting the curve to device data, and B represents half of the peak-to-peak amplitude of the AC flux. Thus, the core loss for the inductors is computed as indicated in:

$$P_{L\_Co} = l_{e_1} A_{e_1} \Delta P_{L_1\_Co} + l_{e_2} A_{e_2} \Delta P_{L_2\_Co} \quad (25)$$

In this case, l_e stands for the length of the magnetic path, and A_e indicates the core's cross-sectional area. Consequently, the overall power loss in the inductor, which includes both core and copper losses, is determined as outlined in:

$$P_L = P_{L\_C} + \Delta P_{L\_Co} \quad (26)$$

The power loss in the capacitor arises from its parasitic resistance r_c. By analyzing the instantaneous current at different operating phases, the approximate RMS value of the current through the capacitors can be computed using:

$$I_{C_{1}(RMS)} = \sqrt{\frac{1}{T}\left(\int_0^{DT} i_{L_2}^2\,dt + \int_{DT}^T i_{L_1}^2\,dt\right)} \approx \sqrt{\frac{D^2-D+1}{1-D}} I_o \quad (27)$$

$$I_{C_{o}(RMS)} = \sqrt{\frac{1}{T}\left(\int_0^T \left(i_{L_2} - I_o\right)^2 dt\right)} \approx \frac{\Delta i_{L_2}}{2\sqrt{2}} \approx \frac{(2-D)DV_{in}}{2\sqrt{2} f_s L_2} \quad (28)$$

Therefore, the power dissipation in the capacitors can be determined using:

$$P_C = I_{C_1(RMS)}^2 r_{C_1} + I_{C_o(RMS)}^2 r_{C_o} = \frac{(D^2-D+1)P_o}{(1-D)R} r_{C_1} + \left(\frac{(2-D)DV_{in}}{2\sqrt{2} f_s L_2}\right)^2 r_{C_o} \quad (29)$$

The primary sources of power loss include conduction losses due to the on-resistance and switching losses during activation and deactivation periods. The conduction losses depend on the on-resistance and the RMS current flowing through the MOSFET. To estimate the RMS current through the switches, (30) and (31) can be used based on the current values observed during different operating conditions:

$$I_{S_{1}(RMS)} = \sqrt{\frac{1}{T}\int_0^{DT}\left(i_{L_1} + i_{L_2}\right)^2 dt} \approx \frac{\sqrt{D}}{1-D} I_o \quad (30)$$

$$I_{S_{2}(RMS)} = \sqrt{\frac{1}{T}\int_0^{DT} i_{L_2}^2\,dt} \approx \sqrt{D} I_o \quad (31)$$

Hence, the conduction losses associated with the switches can be calculated using:

$$P_{S_C} = I_{S_1(RMS)}^2 r_{DS_1} + I_{S_2(RMS)}^2 r_{DS_2} = \left(\frac{D r_{DS_1}}{(1-D)^2} + D r_{DS_2}\right)\frac{P_o}{R} \quad (32)$$

The switching losses of the converter are determined by:

$$P_{S_S} = \frac{V_{S_1} I_{S_1}\left(t_{r_1} + t_{f_1}\right) f}{2} + \frac{V_{S_2} I_{S_2}\left(t_{r_2} + t_{f_2}\right) f}{2} = \left(\frac{f(t_{r_1}+t_{f_1})}{2(1-D)(2-D)} + \frac{f(t_{r_2}+t_{f_2})}{2}\right) P_o \quad (33)$$

The overall power dissipation in the electrical switches comprises both conduction and switching losses, as outlined in:

$$P_S = P_{S\_C} + P_{S\_S} \quad (34)$$

The primary sources of power loss in the diode stem from the forward voltage drop V_F and the series resistance r_D. The approximate RMS value of the current flowing through the diodes, based on an analysis of the instantaneous current during different operating stages, can be calculated using:

$$I_{D_{1}(RMS)} = \sqrt{\frac{1}{T}\int_{DT}^T i_{L_1}^2\,dt} \approx \frac{D}{\sqrt{1-D}} I_o \quad (35)$$

$$I_{D_{2}(RMS)} = \sqrt{\frac{1}{T}\int_{DT}^T i_{L_2}^2\,dt} \approx \sqrt{1-D} I_o \quad (36)$$

Therefore, the expression for the power loss in the diodes can be determined by:

$$P_D = I_{D_1} V_{F_1} + I_{D_2} V_{F_2} + I_{D_1(RMS)}^2 r_{D_1} + I_{D_2(RMS)}^2 r_{D_2} = \left(\frac{DV_{F_1}}{V_o} + \frac{(1-D)V_{F_2}}{V_o} + \frac{D^2 r_{D_1}}{(1-D)R} + \frac{(1-D) r_{D_1}}{R}\right) P_o \quad (37)$$

I. Determine the Efficiency of the Converter

The total power loss of the proposed converter is the sum of the power losses in the inductor, capacitor, switches, and diodes, as determined by:

$$P_{Loss} = P_L + P_C + P_S + P_D \quad (38)$$

As a result, the efficiency of the designed converter can be estimated using the method outlined in:

$$\eta = \frac{P_o}{P_o + P_L + P_C + P_S + P_D} \quad (39)$$

III. COMPARISON WITH OTHER BUCK-BOOST CONVERTER CONFIGURATIONS

As evidenced in Table I, the proposed converter demonstrates superior performance compared to the existing converters documented in the literature. The stress voltage

coefficient for power switch S_1 is lower than the converters in [12-16], and for S_2, it is lower than all other converters except the one in [17]. The ratio for diode D_1 is superior to those in [12, 14-16] and higher than in [12, 17-19]. As for diode D_2, most converters have similar stress ratios except for the configurations proposed in [17, 19]. In DC-DC converters, the normalized stress voltage coefficient is defined as the ratio of the stress voltage on the power switch to the output voltage. This coefficient provides insight into the extent to which the voltage on the power switch exceeds the output voltage, offering a measure of the converter's performance. It is a critical metric for evaluating the efficiency and durability of the converter. A lower stress voltage coefficient is indicative of enhanced operational efficiency and reduced electrical stress for the power switch, which in turn leads to improved performance and extended component longevity.

TABLE I. COMPARISON OF NORMALIZED STRESS VOLTAGES ON SEMICONDUCTOR COMPONENTS WITH A VOLTAGE GAIN RATIO OF 2

Ref	$\frac{V_{S_1}}{V_O}$	$\frac{V_{S_2}}{V_O}$	$\frac{V_{D_1}}{V_O}$	$\frac{V_{D_2}}{V_O}$	D
[12]	$\frac{1-D}{D^2}=1.25$	$\frac{1}{D}=1.72$	$\frac{1-D}{D^2}=1.25$	$\frac{1}{D}=1.72$	0.58
[13]	$\frac{1}{D^2}=2.97$	$\frac{1}{D}=1.72$	$\frac{1-D}{D^2}=0.82$	$\frac{1}{D}=1.72$	0.58
[14]	$\frac{1-D}{D^2}=1.25$	1	$\frac{1-D}{D^2}=1.25$	$\frac{1}{D}=1.72$	0.58
[15]	$\frac{1-D}{D^2}=1.25$	$\frac{1}{D}=1.72$	$\frac{1-D}{D^2}=1.25$	$\frac{1}{D}=1.72$	0.58
[16]	$\frac{1-D}{D^2}=1.25$	$\frac{1}{D}=1.72$	$\frac{1-D}{D^2}=1.25$	$\frac{1}{D}=1.72$	0.58
[17]	$\frac{1-D}{D}=1$	$\frac{2D-1}{D}=0$	$\frac{1-D}{D}=1$	1	0.5
[18]	$\frac{1-D}{D}=1$	$\frac{1}{D}=2$	$\frac{1-D}{D}=1$	$\frac{1}{D}=2$	0.5
[19]	$\frac{1-D}{D}=1$	1	$\frac{1-D}{D}=1$	1	0.5
Proposed	$\frac{1}{2D-D^2}=1.21$	$\frac{1-D}{2D-D^2}=0.51$	$\frac{1}{2D-D^2}=1.21$	$\frac{1}{D}=1.72$	0.58

Similarly, Table II demonstrates the proposed converter configuration's superiority through the components' stress level indices under specific conditions. Specifically, for power switch S_1, this index is lower than the compared configurations, except for the converter configuration in [18]. This superiority is demonstrated through the lowest stress current indices for components S_2, D_1, and D_2 of the proposed converter compared to the configurations studied in [12-19]. This indicates that components in the circuit, such as switches and diodes, experience less stress during operation. This results in higher performance, longer component life, and better heat dissipation, increasing system reliability and stability.

IV. EXPERIMENTAL RESULTS

A practical circuit model, as presented in Figure 6, was implemented to analyze and evaluate the proposed buck-boost converter. In the experiment, a switching frequency of 40 kHz was used, with inductors L_1 and L_2 rated at 0.4 mH and capacitors C_2 and C_o having a capacitance of 47 uF. In practical applications, adding an input filter to DC-DC converters is essential to protect sensitive electronic components from Electromagnetic Interference (EMI) and ensure stable input power, thereby improving the converter's performance and longevity. An input filter helps minimize EMI and ripple on the input power, preventing interference from affecting the power supply and protecting other electronic devices. Consequently, a small filter was proposed with a capacitor value $C_{filter} = 100\,\mu\text{F}$ and an inductor value $L_{filter} = 0.08\,\text{mH}$, connected at the input of the proposed converter

TABLE II. COMPARISON OF NORMALIZED STRESS CURRENTS ON SEMICONDUCTOR COMPONENTS WITH A VOLTAGE GAIN RATIO OF 2

Ref	$\frac{I_{S_1}}{I_{in}}$	$\frac{I_{S_2}}{I_{in}}$	$\frac{I_{D_1}}{I_{in}}$	$\frac{I_{D_2}}{I_{in}}$	D
[12]	1	$\frac{1-D}{D}=0.72$	$\frac{1-D}{D}=0.72$	$\left(\frac{1-D}{D}\right)^2=0.52$	0.58
[13]	1	$\frac{1-D}{D}=0.72$	$\frac{1-D}{D}=0.72$	$\left(\frac{1-D}{D}\right)^2=0.52$	0.58
[14]	1	$\frac{2D-1}{D}=0.28$	$\frac{2D-1}{D}=0.28$	$\left(\frac{1-D}{D}\right)^2=0.52$	0.58
[15]	1	$\frac{1-D}{D}=0.72$	$\frac{1-D}{D}=0.72$	$\left(\frac{1-D}{D}\right)^2=0.52$	0.58
[16]	1	$\frac{1-D}{D}=0.72$	$\frac{1-D}{D}=0.72$	$\left(\frac{1-D}{D}\right)^2=0.52$	0.58
[17]	$2-D=1.5$	$1-D=0.5$	$\frac{1-D}{D}=1$	$\frac{(1-D)^2}{D}=0.5$	0.5
[18]	$D=0.5$	$1-D=0.5$	$1-D=0.5$	$\frac{(1-D)^2}{D}=0.5$	0.5
[19]	1	$1-D=0.5$	$\frac{1-D}{D}=1$	$\frac{(1-D)^2}{D}=0.5$	0.5
Proposed	$\frac{1}{2-D}=0.7$	$\frac{1-D}{2-D}=0.3$	$\frac{1-D}{2-D}=0.3$	$\frac{(1-D)^2}{D(2-D)}=0.21$	0.58

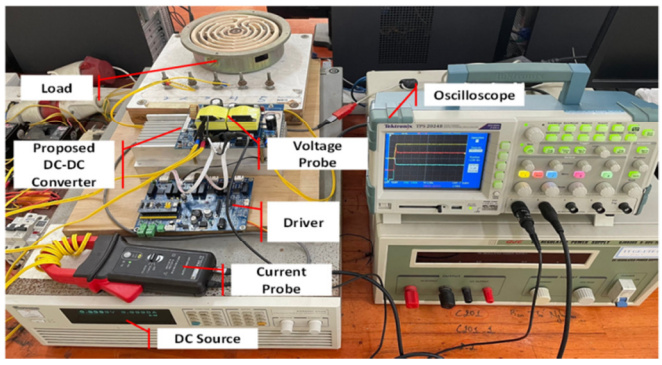

Fig. 6. Experimental model.

Figures 7 and 8 show the experimental results of the proposed converter operating in boost mode, with a DC input voltage of 24 V, a load resistance of $R = 64\,\Omega$, and a switch duty cycle of 60%. Figure 7 also displays an input current ripple (ΔI_{in}) of approximately 50 mA (1.78% of the total input current), while Figure 8 indicates an output current ripple (ΔI_{out}) of approximately 40 mA (2.82% of the total output current). The power dissipation across the components is $4.01W$ (about 5.97% of the input power). Figures 9 and 10 depict the experimental results of the converter at DC voltage $V_{in} = 110\,\text{V}$, $R = 64\,\Omega$, duty cycle of 30% for the switches.

Figure 9 demonstrates that the input current ripple, ΔI_{in}, is approximately 110 mA (or 8.52% of the total input current), while Figure 14 indicates that the output current ripple, ΔI_{out}, is around 100 mA (or 5.74% of the total output current). The power dissipation across the components is 5.31 W, about 3.74% of the input power. Figures 11 and 12 show the experimental results of the proposed converter operating in boost mode with 24 V input, and step-down mode with 110 V input. Figure 13 displays the experimental investigation of the converter operating in both boost and buck modes. The DC input voltage is 24 V, while the duty cycle of the switching gate is varied from 5% to 80%.

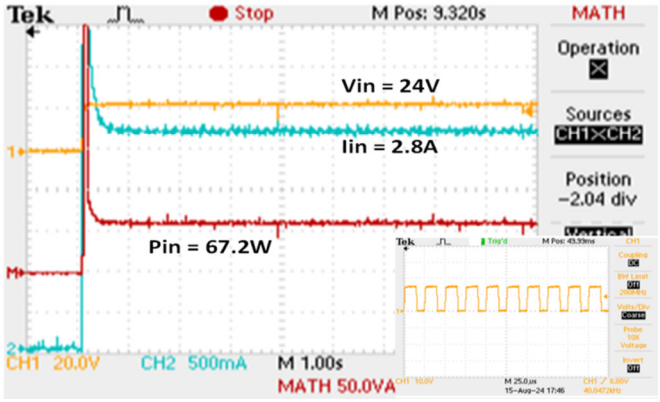

Fig. 7. Waveforms of input current, voltage, and power in boost mode.

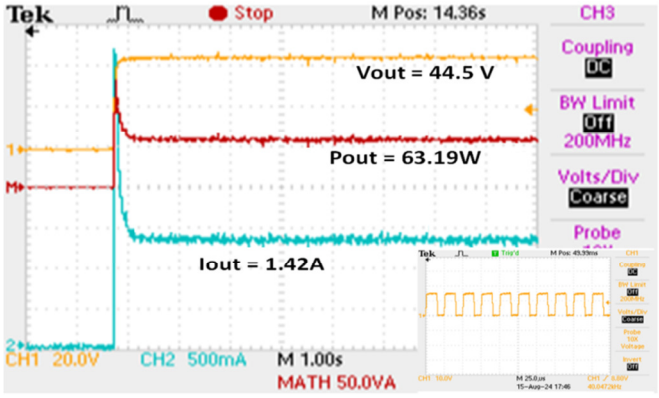

Fig. 8. Waveforms of output current, voltage, and power in boost mode.

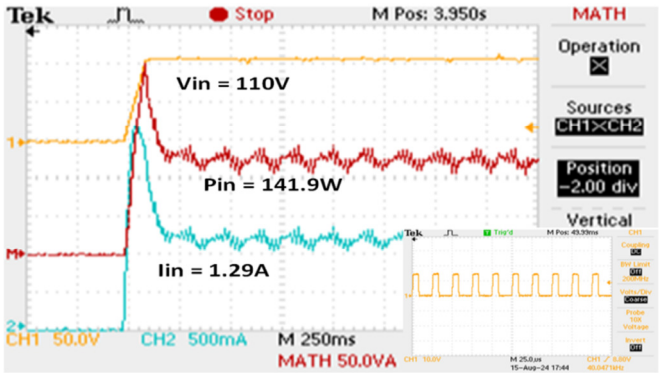

Fig. 9. Waveforms of input current, voltage, and power in buck mode.

Figure 14 portrays the converter's efficiency under the conditions described in Figure 13. The converter exhibits the lowest efficiency at a duty cycle of 5%, achieving 80.53%. However, authors in [20 -22] suggest that DC-DC converters should operate around a duty cycle of 0.5, with operational ranges from $0.1 < D < 0.8$. Thus, the low operational range is rarely used in practice. The fact that the converter's efficiency is below 92% in this range has a minimal impact on practical applications. In the more frequently used operational range ($0.11 < D < 0.73$), the converter's efficiency exceeds 92%, and particularly in the range with an amplifier ratio of less than 3, the converter achieves the highest efficiency of up to 99.16%.

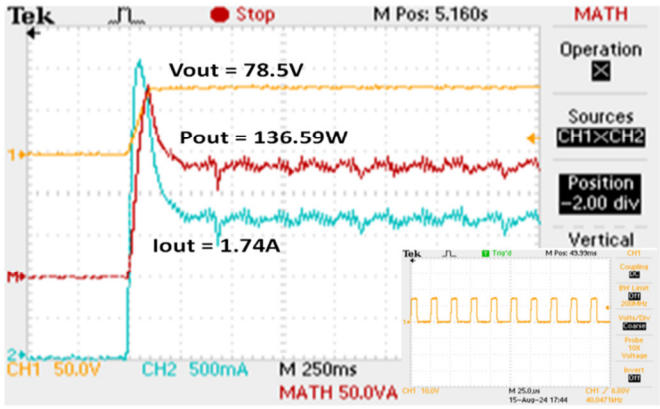

Fig. 10. Waveforms of output current, voltage, and power in buck mode.

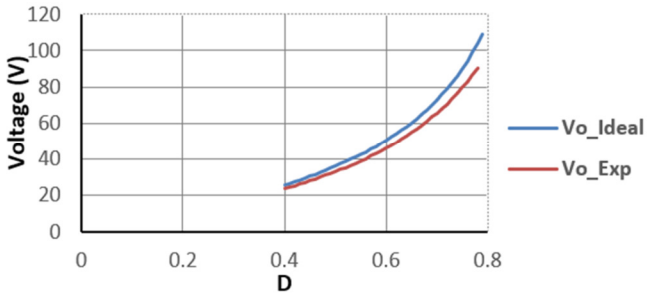

Fig. 11. Output voltage of the proposed converter in boost mode with $V_{in} = 24$ V.

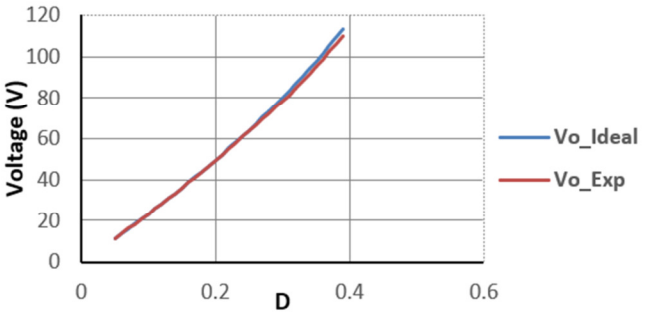

Fig. 12. Output voltage of the proposed converter in buck mode with $V_{in} = 110V$.

V. CONCLUSIONS

This study has proposed, evaluated, analyzed, and experimentally tested a new boost-buck converter. It presents a detailed theoretical analysis of the steady state and comparisons with other positive output converters. Power loss is analyzed to calculate efficiency. The results from theoretical calculations and experiments show consistency and demonstrate that the proposed converter not only provides positive output voltage, but also offers suitable voltage step-up/down capability (V_o/V_i ratio with $D = 0.1 \div 0.8$ exhibits low nonlinearity - Figure 1, within a voltage gain range of < 6). Additionally, with a boost range of less than 3, the proposed converter performs better in terms of lower current and voltage stress than the reviewed studies. Practical experiments also display promising results, with the input current ripple ranging from a minimum of 40 mA to a maximum of 110 mA, and the output current ripple ranging from a minimum of 40 mA to a maximum of 100 mA in the presented test cases.

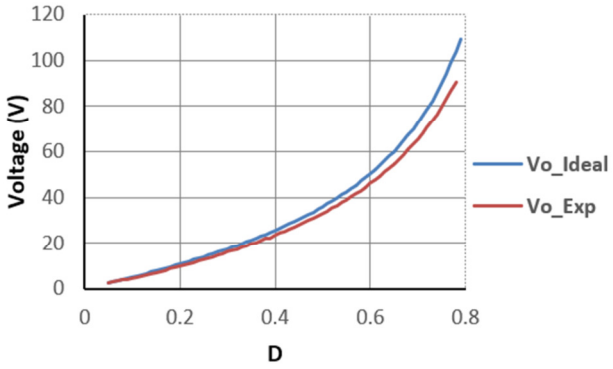

Fig. 13. Voltage conversion ratio of the proposed converter in boost-buck mode.

The analysis and evaluation of the experimental results indicate that the proposed buck-boost converter structure exhibits a superior D adjustment range (with experimental operation performing well within $D = 0.1 \div 0.8$) and a V_o/V_i characteristic with diminished nonlinearity in comparison to DC-DC buck-boost converters with an identical number of switches, inductors, and capacitors. Therefore, the implementation of control methodologies to ensure the maintenance of the output voltage will result in enhanced efficiency and stability. The converter demonstrates excellent voltage regulation, with a nearly linear V_o/V_i ratio in Buck mode and the capacity to achieve up to a sixfold voltage gain in Boost mode with D=0.8 while maintaining optimal voltage regulation. It can thus be concluded that the proposed DC-DC buck-boost circuit will prove highly effective and optimal for devices requiring voltage step-up/down, offering a maximum voltage gain of 6 and good output voltage control capability.

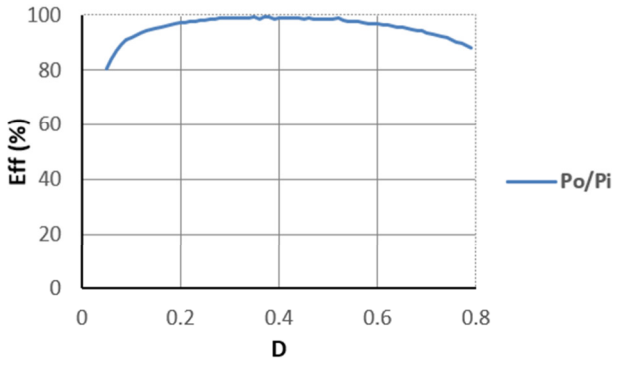

Fig. 14. Evaluation of the proposed converter's power (converter efficiency).

The proposed converter exhibits superior performance in buck mode when the duty cycle (D) is between 0 and 0.4, demonstrating a nearly linear voltage gain that simplifies the implementation of Proportional–Integral–Derivative (PID) control. While other converters display superior performance in boost mode ($0.4 < D < 0.8$), they tend to exhibit instability due to nonlinearity. The proposed converter demonstrates reduced nonlinearity, facilitating more precise control and enhanced stability. The optimal voltage gain ensures smooth operation although improper usage could potentially lead to component damage due to overload.

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