Simplified Carrier-based PWM for Three-Level Transformer-Less Grid-connected Photovoltaic Inverters

Arsalan Ansari
Department of Electronics Engineering, Dawood University of Engineering and Technology, Karachi, Pakistan
dr.arsalanansari@duet.edu.pk (corresponding author)

Muhammad Dawood Idrees
Department of Industrial Engineering and Management, Dawood University of Engineering and Technology, Karachi, Pakistan
muhammad.dawood@duet.edu.pk

Atif Jamil
Department of Computer System Engineering, Dawood University of Engineering and Technology, Karachi, Pakistan
atif.jamil@duet.edu.pk

Abdul Sami
Department of Electronics Engineering, Dawood University of Engineering and Technology, Karachi, Pakistan
dr.abdulsami@duet.edu.pk

Ramesh Kumar
Department of Computer System Engineering, Dawood University of Engineering and Technology, Karachi, Pakistan
ramesh.kumar@duet.edu.pk

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ABSTRACT

This article proposes a simple and efficient carrier-based Pulse Width Modulation (PWM) technique for three-level transformer-less grid-connected Photovoltaic (PV) inverters. The three-level inverter is prone to an inherent issue of unbalanced DC-link voltages, which, when used in conjunction with transformer-less grid-connected PV systems, gives rise to leakage currents. A simplified carrier-based PWM is proposed to carry out the DC-link voltage balancing and suppress the leakage current, i.e. Common Mode (CM) current, in transformer-less grid-connected inverters. The implementation of the proposed strategy is straightforward and does not require complex calculations, in contrast to space vector-based PWM techniques or multi-carrier modulation techniques. The operation of the PWM strategy is demonstrated through simulations and validated through experimental results.

Keywords-carrier-based PWM; grid-connected inverters; photovoltaic

I. INTRODUCTION

In PV applications, the primary considerations are the scale, cost, and efficiency of the PV generation. Accordingly, transformer-less three-level inverters are employed for the purpose of connecting PV arrays to the grid [1-3]. Nevertheless, transformer-less three-phase three-level inverters facilitate the flow of leakage current through the parasitic capacitances [4] of the PV array to the ground. Moreover, three-level inverters are susceptible to DC-link voltage unbalance. These issues may result in the generation of harmonics, increased losses, electromagnetic interference, and

potential electrical safety concerns in grid-connected inverters [5, 6]. Therefore, it is imperative to identify solutions to address these challenges. There is a notable absence of literature addressing these issues in a simultaneous manner. Nevertheless, a substantial body of research has been carried out to deal with these issues on an individual basis. A number of modulation strategies have been proposed in the literature as a means of eliminating leakage currents. Authors in [7] and [8] employed space vector PWM methods to address the issue of leakage current through the use of appropriate space vector combinations. Authors in [9] put forth a three-phase, three-level inverter configuration that incorporates supplementary components and a DC-DC step-up converter stage preceding the three-phase inverter stage. The switching of the DC-DC step-up converter is coordinated with that of the inverter, which serves to eliminate the CM current. The incorporation of additional components and the boost of converters prior to the inverter stage results in a more complex configuration and, despite this, remains cost-effective. Additionally, authors in [10] proposed a method for capacitor voltage balancing in T-type neutral point clamped inverters that incorporates additional circuitry with the inverter. In a further contribution to the field, authors in [11] proposed a combination of two different space vector PWM techniques to address both leakage current and DC-link voltage balancing issues. Nevertheless, given the intricate calculations and profound comprehension involved, a carrier-based PWM is invariably preferable to a space vector PWM. Authors in [9] and [10] presented a carrier-based PWM for a three-level inverter. In the first case, the phase-disposed carrier results in the employment of only a two medium-voltage (CM voltage) and a zero-voltage vector during one switching period. In the second case, the phase-opposition disposed carrier results in the use of solely three medium-voltage vectors to suppress leakage current. However, the authors did not address the issue of DC-link voltage unbalancing. This article proposes a simple carrier-based PWM for a three-level grid-connected inverter that employs a single carrier for the operation of a three-level inverter. The proposed method is demonstrated to suppress the CM current and balance the capacitor voltages.

The proposed strategy is based on the operation of a single carrier with a three-level inverter. The three-level inverter is typically operated in conjunction with multiple carriers and their combinations. The use of a single carrier to control the operation of a three-level inverter facilitates the implementation of a more straightforward control system. Moreover, the proposed strategy employs two medium vectors and a zero vector during a switching period of the three-level inverter, simultaneously mitigating leakage current and Neutral-Point (NP) voltage imbalance. The employment of medium vectors for the operation of the inverter maintains a constant common mode voltage throughout the inverter's operational lifespan, thereby mitigating the leakage current. Given the nature of the triangular carrier, the medium vectors are employed in a manner that ensures that the application of the two medium vectors during a switching period is sufficient to facilitate the balancing of the NP voltage. It would appear that, as far as is known, neither the leakage current nor the NP voltage balancing problem have been addressed in the literature simultaneously. The proposed carrier-based PWM strategy was subjected to simulations and experiments. The results substantiate the theoretical analyses and demonstrate the practical viability of the proposed PWM strategy.

II. NOVEL CARRIER BASED PWM

The configuration of the transformer-less grid-connected three-level Neutral Point Clamped (NPC) inverter is shown in Figure 1. The capacitance C_{pv}, which is connected to each PV array, is defined as the parasitic capacitance. This capacitance varies with numerous environmental parameters, where Rg is the ground resistance, E_i, $i = (a, b, c)$, is the grid phase voltage, and R and L are the interfaced reactor's resistance and inductance, respectively. Each inverter phase leg is composed of four switches and can be connected to either P ($V_{dc}/2$), O (0), or N ($-V_{dc}/2$) by appropriately activating or deactivating the switches (S_{xi}, $x = (a, b, c)$, $i = (1\text{-}4)$), as indicated in Table I. Consequently, a total of 33 switching states for a three-level inverter are possible, as portrayed in Figure 2.

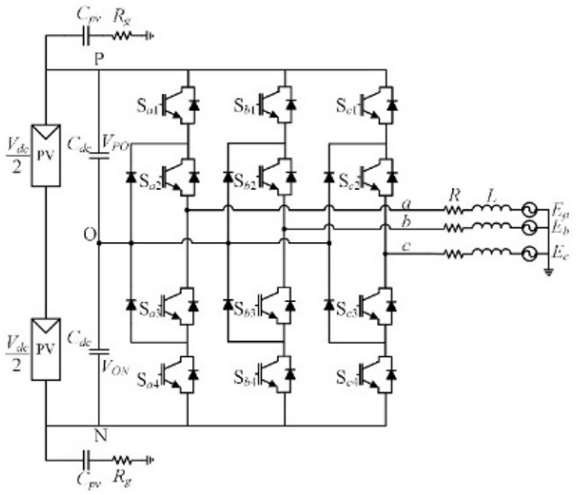


Fig. 1. Transformer-less grid connected three-level NPC inverter with PV as the input.

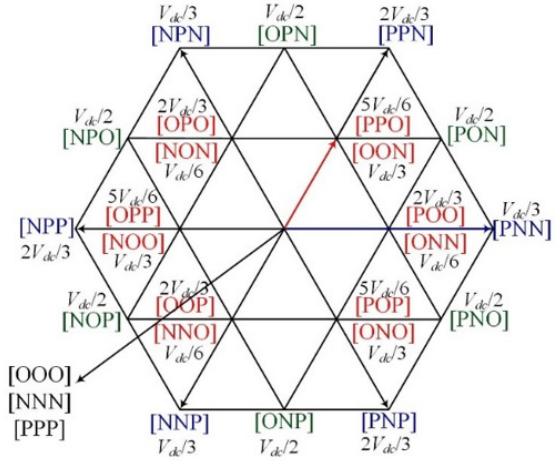


Fig. 2. Space vector (switching states) and corresponding CM voltage of three-level inverter [12].

TABLE I. SWITCH STATUS AND OUTPUT VOLTAGE OF ANY LEG OF THREE- LEVEL INVERTER

Switching State/Switching function (S_x)	Switching Device Status				Output
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	
P/1	1	1	0	0	$V_{dc}/2$
O/0	0	1	1	0	0
N/-1	0	0	1	1	$-V_{dc}/2$

The corresponding CM voltages as defined by (1), [13]:

$$V_{CM} = \left(\frac{V_{aN}+V_{bN}+V_{cN}}{3}\right) \quad (1)$$

where V_{aN}, V_{bN} and V_{cN} are the output voltages of phase *a*, phase *b* and, phase *c,* respectively with regard to the neutral point *N*. The CM current in transformer-less grid connected PV systems is strongly dependent on C_{pv} and V_{CM}, as given by (2):

$$i_{leakage} = C_{pv}\frac{dV_{CM}}{dt} \quad (2)$$

If V_{CM} is kept constant, the leakage current would be theoretically zero. It is evident from Figure 2 that the switching states [*PON*], [*OPN*], [*NPO*], [*NOP*], [*ONP*], [*PNO*], and [*OOO*] produce the same magnitude of V_{CM}, which is $V_{dc}/2$. As an example, for [*PON*] switching state $V_{aN} = V_{dc}$, since for this switching state phase *a* is connected to *P*, similarly $V_{bN} = V_{dc}/2$ and $V_{cN} = 0$, and thus $V_{CM} = \frac{\left(V_{dc}+\frac{V_{dc}}{2}+0\right)}{3} = \frac{V_{dc}}{2}$. Therefore, by employing all these vectors in a PWM technique, the CM voltage can remain unchanged, and consequently CM current can vanish in transformer-less grid connected PV systems. In order to achieve the previously described objective of maintaining a constant CM voltage, Figure 3 presents the block diagram of a novel carrier-based PWM strategy. In this strategy, the three-phase reference carriers, a, b, and c, are used. The zero-sequence signal (V_{ZSS}) is given by (3):

$$V_{ZSS} = \begin{cases} 1 - max(a,b,c), & if\ V_x \geq 0 \\ -1 - min(a,b,c), & otherwise \end{cases} \quad (3)$$

where $V_x = max\ (a, b, c) + min\ (a, b, c)$.

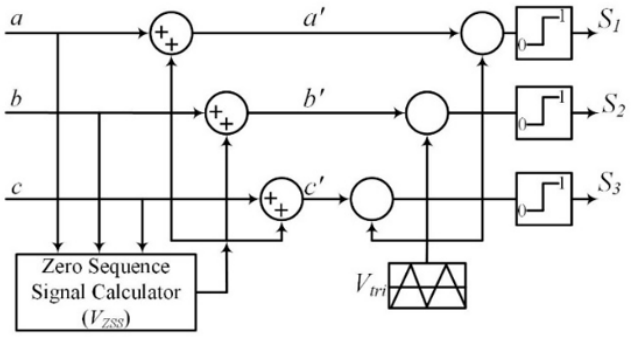


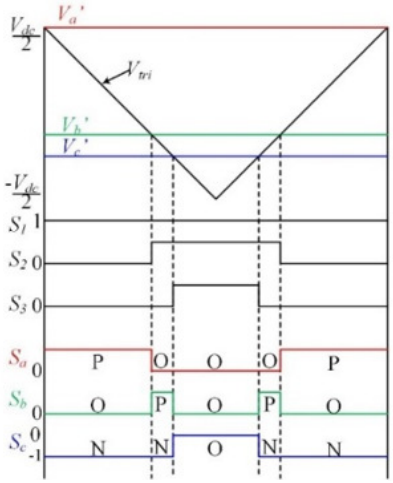
Fig. 3. Block diagram of new carrier-based PWM.

The V_{ZSS} is included in the reference carrier and the modified reference signals obtained are *a'*, *b',* and *c'*, which are then measured against a single triangular carrier V_{tri} to obtain intermediate signals S_i, where (i =1, 2, 3) is given by (4):

$$S_i = \begin{cases} 1, & if\ x' \geq V_{tri} \\ 0, & otherwise \end{cases} \quad (4)$$

The switching function S_x, where $x = (a, b, c)$, represents the switching state of the corresponding phase, and is obtained in terms of S_1, S_2, and S_3 as $S_a = S_1 - S_2$, $S_b = S_2 - S_3$, and $S_c = S_3 - S_1$. The switching function S_x may take the values of 1, 0 or -1, depending upon the values of S_1, S_2, and S_3, accordingly. The gating signals for the switches of three-level inverter can be obtained as given by Table 1. Figure 4 presents the relationship between the proposed carrier-based strategy and the space vectors of the three level NPC inverter. The intermediate signals, switching function, and the space vectors used during a particular switching period, are shown. Only vectors [PON], [OPN], and [OOO] -the shaded area of Figure 4 (b)- are deployed during this switching interval to produce constant CM voltage of $V_{dc}/2$. Therefore, this must result in the mitigation of the leakage current according to (2).

(a)



(b)

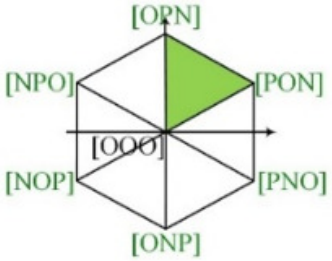


Fig. 4. Relationship between space vectors -shaded area of (b)- with new carrier-based PWM.

III. SYSTEM MODEL

The system depicted in Figure 1 can be displayed in a similar manner to that shown in Figure 5. In this configuration, the three-level inverter is replaced by the CM voltage of each phase with respect to terminal *N*, which is, v_{aN}, v_{bN}, and v_{cN}. The resistance *R* is assumed to be negligible and is therefore omitted from the model. The impedance $Z_{leakage}$ is composed of the parasitic capacitance C_{pv} and R_g. The model is a resonant

circuit, and R_g is a crucial parameter to consider as it influences the damping of the resonant circuit. The transfer function can be derived using the methodology introduced by authors in [14]:

$$H(s) = \frac{i_{leakage}(s)}{v_{CM}(s)} \quad (5)$$

where $i_{leakage}$ can be obtained as:

$$i_{leakage} = \frac{v_{CM}(s)}{R_g + Ls/3 + 2/C_{pv}s} \quad (6)$$

By rearranging the transfer function, $H(s)$, it is possible to obtain the following result:

$$H(s) = \frac{3C_{pv}s}{LC_{pv}s^2 + 3R_gC_{pv}s + 6} \quad (7)$$

MATLAB was employed to generate the bode plot of the transfer function indicated in (7), and the resulting data are presented in Figure 6. This describes the impact of varying values of R_g on the damping effect. In order to achieve a minimal damping effect, the value of R_g was selected to be 5 Ω.

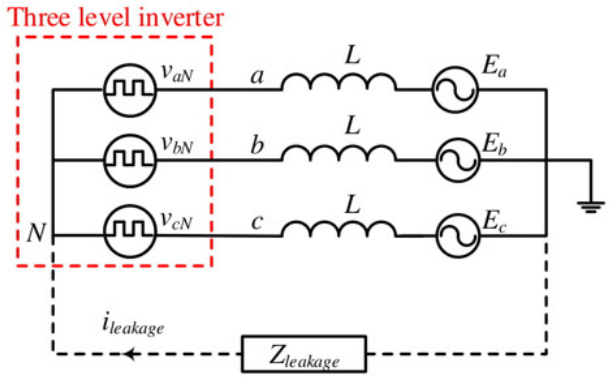


Fig. 5. Model of the three-level grid-connected inverter.

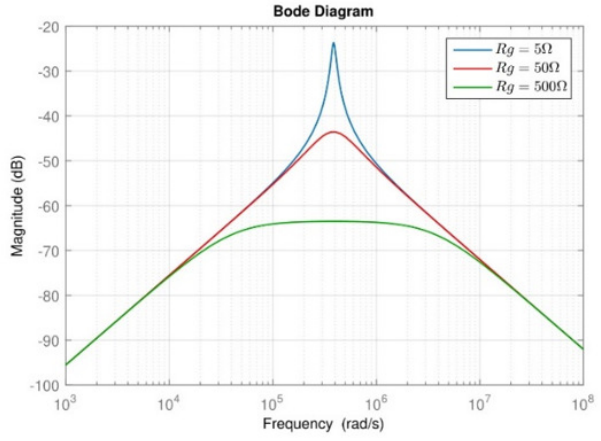


Fig. 6. Effect of ground resistance (R_g) on damping.

IV. SIMULATION RESULTS

In order to assess the efficacy of the recently developed carrier-based PWM, a series of simulations have been conducted using Physical Security Information Management (PSIM) software. To streamline the simulations, the PV array is represented as a constant DC source, and the capacitance C_{pv} is depicted as a constant capacitance connected to both terminals of the PV array. The typical value of C_{pv}, as cited by authors in [15], is 3 nF/kW, though this may fluctuate in response to environmental influences. In consideration of the most unfavorable scenario, the value of C_{pv} is selected as 50 nF. The remaining system parameters used in the simulations and experiments are presented in Table II. The results of the simulations are provided in Figures 7 and 8. The current in the CM and the three-phase currents (i_a, i_b, and i_c) with a new carrier-based PWM strategy when the modulation index is set to 0.9 are shown in Figure 7. The calculated RMS value of the CM current is 119.05 mA. The German standard DIN VDE 0126-1-1 establishes limitations regarding the leakage current in grid-connected PV systems, specifying a maximum allowable limit of the leakage current to a mean level of 300 mA. The new carrier-based PWM strategy has been demonstrated to reduce the leakage current to a level that is well below the standardized threshold.

TABLE II. SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters	Values
V_{dc}	300 V
L	400 mH
R	0.1 Ω
E_{ab}, E_{bc}, E_{ca},	110 V rms
C_{pv}	50 nF
R_g	5 Ω
C_{dc}	1,100 µF
f_s	7.5 kHz
Dead time	3 µsec
C_f	40 µF
P	kW

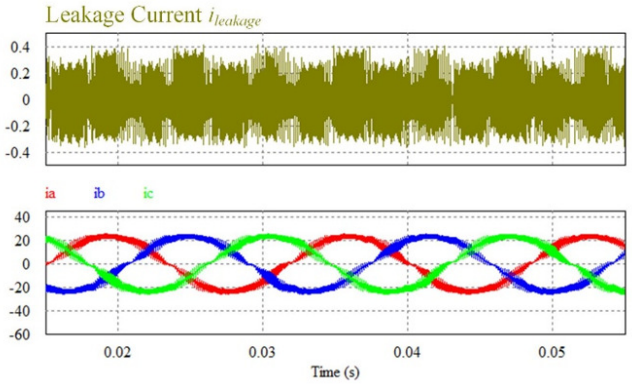


Fig. 7. Leakage current (top) and three phase currents with new carrier-based PWM.

Figure 8 illustrates the pole voltage V_{aO} (top) and line voltage V_{ab} (bottom). Given that the line voltage of a three-level inverter is constituted by five levels, it is essential to note that the line voltage invariably fluctuates between one of the four other levels (all levels are displayed in Figure 2) of line-to-line voltage and zero level. This phenomenon is attributed to

the recurrent utilization of the zero state [OOO] throughout each switching interval.

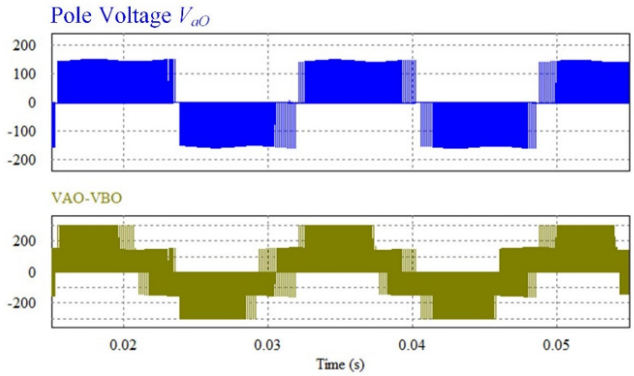


Fig. 8. Pole voltage (V_{aO}) and line voltage of three-level inverter using new carrier-based PWM.

V. EXPERIMENTAL RESULTS

The experiments are conducted in a laboratory setting, and the complete experimental setup is exhibited in Figure 9. The experimental setup includes the following components: an NPC inverter module with control cards, input and output modules, an oscilloscope, filter capacitors, a power stack, and an interfaced reactor. The control of the proposed technique is conducted via a Digital Signal Processor (DSP), specifically the TMS320F28335. Furthermore, dead time is implemented in a Complex Programmable Logic Device (CPLD). The Insulated Gate Bipolar Transistor (IGBT) control signals are derived from the DSP card, which is operated by a computer.

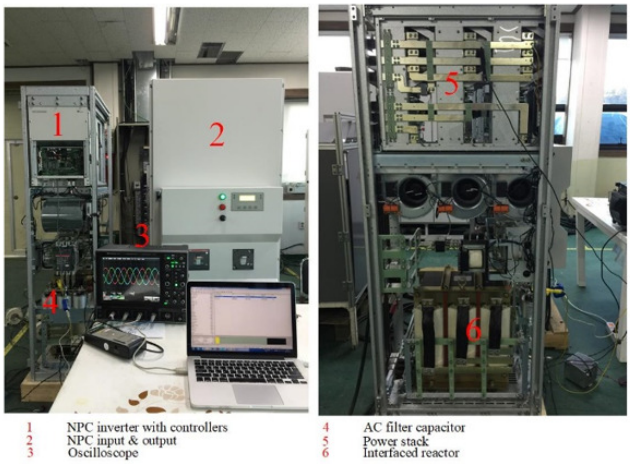


Fig. 9. Experimental setup including power stage and control stage.

The experimental results were obtained under the same conditions as specified in Table II and are in close alignment with the simulation outcomes, as evidenced in Figure 10. The simulation results with regard to the three-phase currents (i_a, i_b, and i_c) and leakage current are verified. The RMS value of the leakage current obtained from the experimental results is 69 mA, which is below the level of 300 mA as specified by the German standard DIN VDE 0126-1-1, while the pole voltage V_{aO} and the line voltage V_{ab} are confirmed. These results demonstrate a high degree of correlation with the simulations, thereby validating the concept of the proposed carrier-based PWM. As previously outlined, the novel carrier-based PWM methodology is also effective in achieving capacitor voltage balancing.

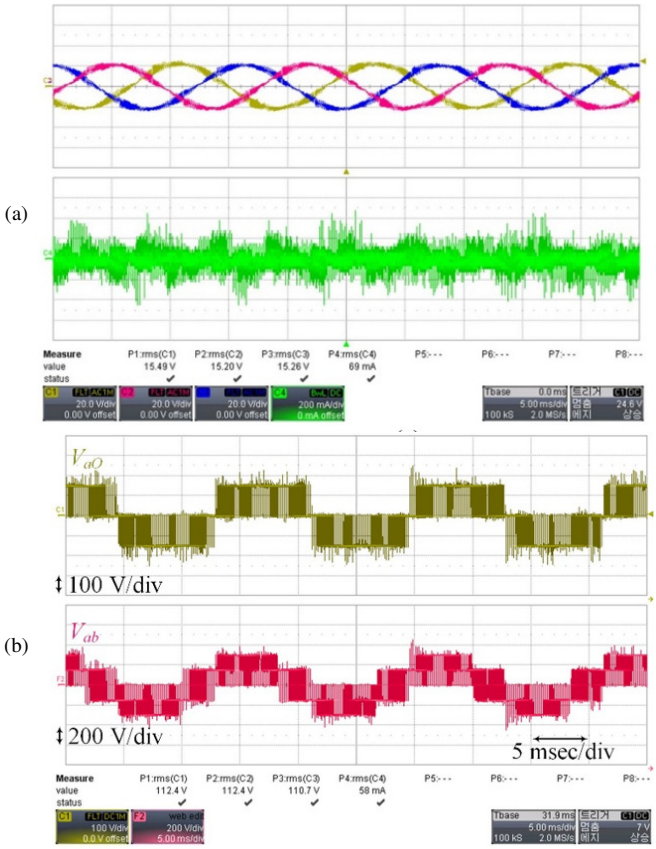


Fig. 10. Experimental results (a) three phases current and leakage current (b) pole voltage and line voltage of three level inverter.

The simulation and experimental validation of the capacitor voltage balancing are portrayed in Figure 11. To analyze the NP voltage balancing, simulations were conducted using PSIM software. The upper capacitor voltage, V_{PO}, was set to 200 V, and the lower capacitor voltage, V_{ON}, was initially adjusted to 100 V. During a switching period, two medium vectors and a zero vector are employed. Given the carrier-based nature of the proposed PWM, the application of the medium vectors is such that the medium vector PON is used for a greater time than the other medium vector OPN. The distribution of the application of the medium vector over time enables this PWM strategy to balance the NP voltage of the three-level inverter. Furthermore, a balanced NP voltage is crucial for the reduction of harmonics at the output. The simulation results for the two capacitor voltages, V_{PO} and V_{ON}, are shown in Figure 11. The recently developed carrier-based PWM is capable of capacitor voltage balancing in approximately 200 milliseconds. Figure 11 (b) presents the experimental results for the two voltages, V_{PO} and V_{ON}. To set the two capacitor voltages at different levels, a 25 kΩ resistor is connected across the upper capacitor and a 15 kΩ resistor is connected across the lower capacitor. The simulation

and experimental results complement each other and carry out DC link voltage balancing in 200 msec.

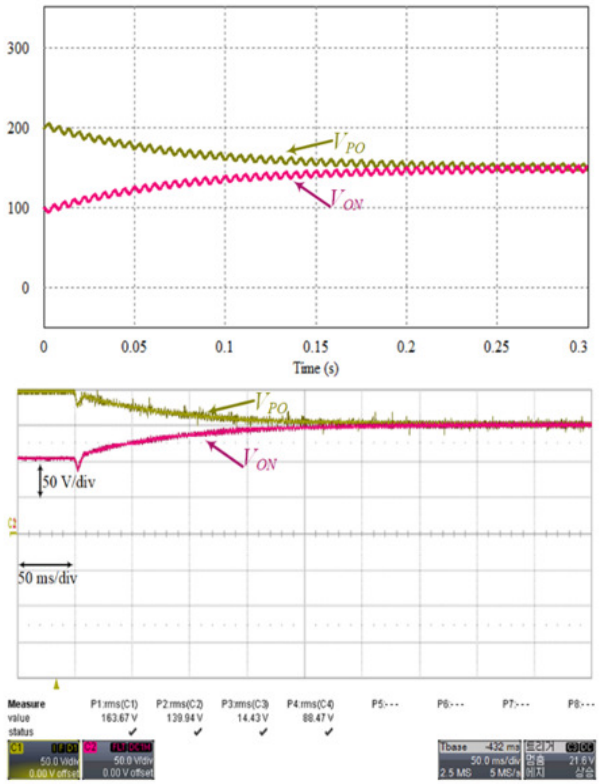


Fig. 11. Simulation and experimental results for the two capacitor voltages, V_{PO} and V_{ON}.

VI. CONCLUSION

A simple, straightforward, and cost-effective carrier-based Pulse Width Modulation (PWM) technique has been presented for three-level grid-connected Photovoltaic (PV) systems. The novel aspect of the proposed PWM technique is that it enables the Common Mode (CM) voltage to be maintained at a constant level by utilizing a single carrier, thereby facilitating the mitigation of CM current and the balancing of DC-link voltages. Additionally, the method's structural simplicity makes it readily adaptable to any digital signal processor. The carrier-based PWM has been subjected to comprehensive investigation through simulations and experiments, and the results have demonstrated its efficacy in maintaining leakage current within acceptable limits.

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