Optimizing Sliding Mode Controller in a DC Microgrid with Variant Constant Power Loads

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ABSTRACT

The optimization of a suitable controlling method is a priority in running any DC/DC boost converter effectively. However, a problem may arise as the occurring oscillations in the microgrid caused by the incremental negative resistance of the Constant Power Load (CPL) variation may lead to system instability. In order to tackle this intrinsic problem, three proposed Sliding Mode Control (SMC) methods were simulated and examined against multiple variations of CPL in MatLab/Simulink. Integral Sliding Mode Control (ISMC) and Two-variable Sliding Mode Control (TSMC) methods showed a better system performance than the Low Pass Filter SMC (LPFSMC) in terms of stability of output voltage in both steady state and transient conditions. The output voltages of ISMC and TSMC had a margin of error of approximately 1 V in the steady-state response and a minor overshoot of less than 1% in the transient response. The steady-state output voltage when using LPFSMC showed approximately 3 V of error and the transient state had a noticeable overshoot near 3%. However, all three controlling methods had a similar efficiency of around 98%. The outstanding robustness of ISMC exhibited the highest voltage stability with the lowest chattering in both steady state and transient responses through the compensation of adequate current to satisfy the CPL requirement.

Keywords-DC microgrid; sliding mode control; boost converter; constant power load; voltage stability

I. INTRODUCTION

The increasing penetration of renewable energy comes from natural resources or processes (e.g. photovoltaic (PV) panels, wind turbines, and fuel cells) that don't emit carbon dioxide and other greenhouse gases [1-3]. A renewable energy-based microgrid (MG) appears as a good solution, taking into consideration exploiting renewable energy and reducing the environmental risks of fossil fuels [4, 5]. The MG system is a network that gives a suitable solution to manage the distribution of sources in the electric power grid, connected Distributed Generation Units (DGUs) using Renewable Energy Sources (RESs), Energy Storage Systems (ESSs), and loads. MGs are classified as DC- or AC-MGs [6]. A DC-MG has the benefit of high performance [7] and may be more useful than the AC-MG, as it is attractive in distribution systems due to the integration of a variety of ESSs such as batteries, super capacitors, etc. [8]. The research community has shifted towards the development of DC-MG as it has high efficiency, reliability, and controllability, supporting various DC loads [9, 10].

The DC-MG performs a multitude of functions like grid stability, power quality provision, and supply-demand balance. DC-MGs contain a number of power electronic converters that interact between distribution sources of different voltage levels and loads [10]. If small variations around the expected output values occur, then the power electronic converters tightly regulate their output voltage causing the whole system to collapse [11]. This converter problem decreases system damping, which leads to critical oscillations, thus producing an uncontrollable and unstable system. Constant-Power Loads (CPLs) have an inverse proportional v-i relationship with a negative incremental impedance, thus introducing a destabilizing effect [12]. Conventional Proportional-Integral-Derivative (PID) controllers are used for linearizing the system around an operating point design, which can only ensure a small signal stability [13]. The large signal stability with non-

linearity of power electronic converters, distribution and generation, as well as load complicate the control system, thus producing a need to develop a better control strategy to reduce the effect of system stability. The Sliding Mode Control (SMC) is an eminent, robust control technique, commonly applied to power converters against system parameter variation. SMC is easy to implement and has fast-transient response [14-17]. The main objective of this work is to propose different SMCs to reduce the high effect stability of power electronics loaded by CPLs based on pulse-width modulation to keep the whole system stable.

The stability of DC-DC power electronic converter systems with CPLs attract the attention of the scientific community. In 2020, authors in [18] proposed hybrid MPC of boost converters with CPLs. They developed an advanced control technique by minimizing a finite-prediction horizon cost function to ensure DC microgrid stability of the hybrid system implemented. Authors in [19] presented a hybrid passivity-based model control for voltage regulation and stabilization in DC MGs with CPLs. They implemented a PI controller and a passivity-based controller to form a hybrid controller to improve the stability of the system and control robustness. Authors in [20] introduced the second-order SMC design of the buck converter with CPLs that used Super Twisting SMC to suppress the chattering effect and maintain robustness under load variations and parametric uncertainties. In 2024, authors in [21] designed the adaptive voltage-guaranteed control of DC/DC-Buck-Converter-Interfaced DC MGs with CPLs to enhance both steady-state and transient performances.

DC-DC boost converters with CPLs have been widely considered in different implemented SMC methods for load sharing and improving transient performance.

II. DESIGN AND METHODOLOGY

A. DC Microgrid

In the DC MG, the devices are connected through power lines to a DC bus consisting of a diesel rectified generator, renewable resources, hybrid ESSs, feeding multiple loads [22, 23]. The multiple loads in the cascaded converter power systems of DC MG are of two types, Constant Voltage Loads (CVLs) and CPLs [24]. It is very essential to manage the stability of the DC bus voltage in order to ensure the stability of the DC MG, Figure 1, displays a circuit diagram of the DC-MG [12]. The outputs of the circuit are tightly regulated by electronics power converters, which behave as CPLs [25]. The characteristic of CPLs is the inverse proportional of *v-i* characteristic and equivalent to a dynamic negative incremental resistance which causes instability in the dc bus [26].

B. Boost Converter with a Constant Power Load (CPL)

The schematic diagram of Figure 2 introduces a simplified DC power system consisting of a DC-DC boost converter and a CPL. In this system, the distributed power supply acts as a constant input voltage source V_{in}. The CPL is connected to the DC bus in parallel, the output voltage of the DC bus is the capacitor voltage V_C, and L is the input inductor. The controllable switch is either MOSFET or IGBT, while the uncontrollable one is the diode. The Continuous Conduction Mode (CCM) operation of the boost converter is in a complementary manner and has two states.

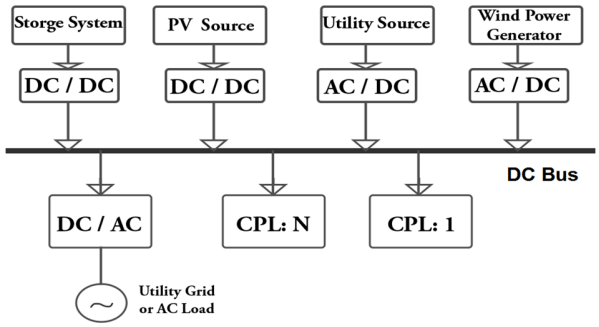

Fig. 1. System model of the DC MG.

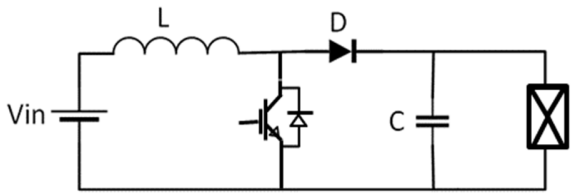

Fig. 2. DC-DC boost converter with a CPL.

State 1 ($0 < t < t_{on}$)

Switch (S1) is ON to charge the inductor (L) and the diode (D) is OFF. The inductor current $i_L(t)$ is greater than zero and ramps up linearly. The voltage across the inductor V_{in} is calculated by:

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_c} \end{bmatrix} = \begin{bmatrix} \frac{1}{L} V_{in} \\ -\frac{1}{C}\frac{P}{V_C} \end{bmatrix} \quad (1)$$

State 2 ($t_{on} < t \leq T_s$)

Switch (S1) is OFF and the diode is ON. The inductor starts to discharge and its current decreases until the switch becomes ON in the next cycle. The inductor voltage is (V_{in}-V_c). The $i_L(t)$ and $V_L(t)$ of State 2 are calculated as:

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_c} \end{bmatrix} = \begin{bmatrix} \frac{1}{L}(V_{in} - V_C) \\ \frac{1}{C}[i_L - \frac{P}{V_C}] \end{bmatrix} \quad (2)$$

where the state space depiction of the ideal switch model is denoted by (3) and the output voltage equation by (4):

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_L} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L}\bar{u} \\ \frac{1}{C}\bar{u} & \frac{-P\bar{u}^2}{C V_{in}^2} \end{bmatrix} \begin{bmatrix} i_L \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in} \quad (3)$$

$$[v_o] = [0\ 1] \begin{bmatrix} i_L \\ V_c \end{bmatrix} \quad (4)$$

C. Sliding Mode Control of Boost Converter

Different SMC methods have been proposed to produce a well stabilized output voltage that operates at fixed frequency, regardless of the nonlinearity of the DC-DC converter, or the

input voltage and load current variations at any operating condition. Designing a suitable sliding surface coefficient of the controller is important for a fast and reliable response. The basic principle of SMC is to design a high speed switching mechanism to utilize the control method with state variables that do not have any ripple and direct the state variables' trajectory toward a desired origin [20]. The system trajectory before reaching a sliding surface stays in a reaching mode called sliding mode. The sliding surface *S* is calculated by [21]:

$$S = Ke + \dot{e} \quad (5)$$

$$Lim\, S.\dot{S} < 0 \quad (6)$$

where *K* represents the coefficients of a sliding surface.

1) Case 1: Two-Variable Sliding Mode Controller (*TSMC*)

TSMC has been proposed for a DC-DC boost converter with two parameters, the current and the voltage of the capacitor as shown in Figure 3.

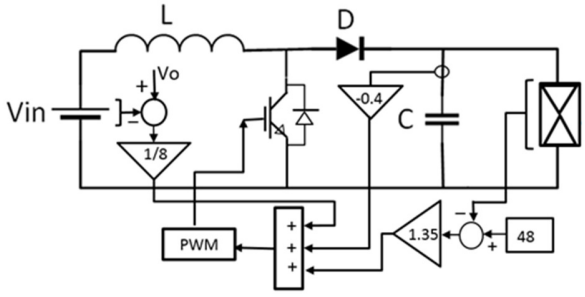

Fig. 3. System model of TSMC.

Using the state-space averaging method [25, 26], the dynamic model of the DC to DC boost converter can be written as:

$$\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & \frac{P}{CVc^2} & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} x_1' \\ x_2' \\ x_3' \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{-\beta(Vo-Vin)}{LC} \\ 0 \end{bmatrix} \bar{u} \quad (7)$$

The sliding surface is introduced as:

$$S = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 \quad (8)$$

where α_1, α_2 and α_3 are the sliding coefficients. The control state variables are: x_1 is the error of a load voltage, x_2 is the rate of the change of the error in the voltage, and x_3 is the integration of voltage error. The state space parameters are described as in (8) [27]. The control law is derived from solving the sliding surface dynamics, once they are in equilibrium.

$$\dot{S} = \alpha_1 \frac{d}{dt}\left(V_{ref} - \frac{\beta}{C}\int i_c \, dt\right) + \alpha_2 \frac{d}{dt}\left(\frac{\beta P}{CV_o} + \frac{\beta}{LC}\int (V_{in} - V_0)\bar{u}\, dt\right) + \alpha_3 \frac{d}{dt}\int \left(V_{ref} - \beta V_0\right) dt \quad (9)$$

The control input variable (u) is defined as [27]:

$$u_{eq} = -\beta L \times \left(\frac{a_1}{a_2} + \frac{\beta P}{CV_o^2}\right) i_c - \frac{a_3 LC}{a_2}(V_{\text{ref}} - \beta V_o) + \beta(V_o - V_i) \quad (10)$$

$$u_{eq} = -K_{p1} i_c - K_{p2}(V_{\text{ref}} - \beta V_o) + \beta(V_o - V_i) \quad (11)$$

$$K_{p1} = \beta L \times \left(\frac{a_1}{a_2} - \frac{\beta P}{CV_o^2}\right) \quad (12)$$

$$K_{p2} = \left(\frac{a_3}{a_2}\right) LC \quad (13)$$

where K_{p1} K_{p2} represent the constant gain for the feedback i_C and $V_{ref} - \beta V_o$, respectively.

2) Case 2: Low Pass Filter Sliding Mode Controller (*LPFSMC*)

In this case, the SMC has two parameters, the current inductor i_L and the output voltage v_C [28, 29] as shown in Figure 4.

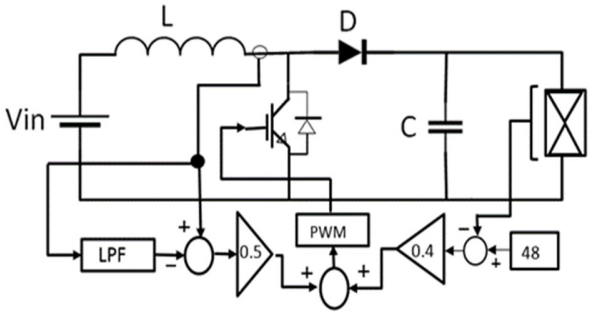

Fig. 4. System model of the LPFSMC.

3) Case 3: Integral Sliding Mode Controller (*ISMC*)

The main idea of the ISMC, as shown in Figure 5, is to guarantee the robustness of the closed-loop system response and to reduce the reaching phase [30].

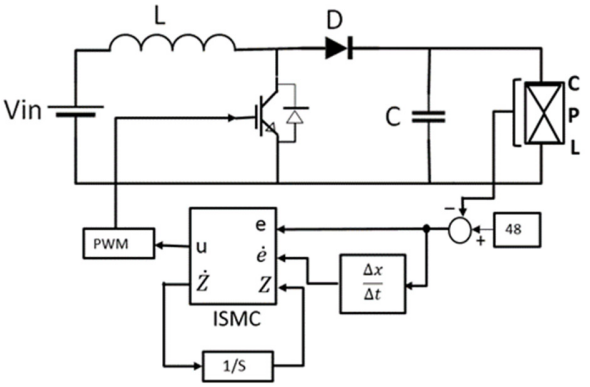

Fig. 5. System model of ISMC.

The integral sliding surface (*S*) that achieves the desired performance and robustness is characterized as in (14):

$$S = \sigma(e) + z(t) \quad (14)$$

$$\sigma(e) = \dot{e} + \lambda e \quad (15)$$

where $z(t)$ is the integral term and $\sigma(e)$ is the linear combination of the system states [30, 31]. The $\dot{z}(t)$ is defined as:

$$\dot{z} = \lambda \dot{e} - \dot{\bar{u}}_0 \quad (16)$$

$$e = V_{ref} + V_o \quad (17)$$

Taking time derivative of (15) and using (16) and (17), we get the sliding surface as defined in (18):

$$\dot{S} = \ddot{e} - \dot{\hat{u}}_0 \quad (18)$$

III. RESULTS AND DISCUSSION

To validate the stability and performance of the considered SMC methods for a CPL and variable input voltages, MATLAB/Simulink software was utilized. The design parameters taken into account for the simulation of DC-DC boost converter were are shown in Table I. The simulated waveforms of inductor's current and output voltage for the DC-DC boost converter with different types of SMC are shown in Figures 6 and 7.

TABLE I. PARAMETERS OF THE DC-DC BOOST CONVERTER

Parameter	Value
Inductance, L	80 µH
Capacitance, C	1600 µF
Output Load, R_L	10 Ω
Input Voltage, V_{in}	30 V
Bus voltage, V_o	48 V

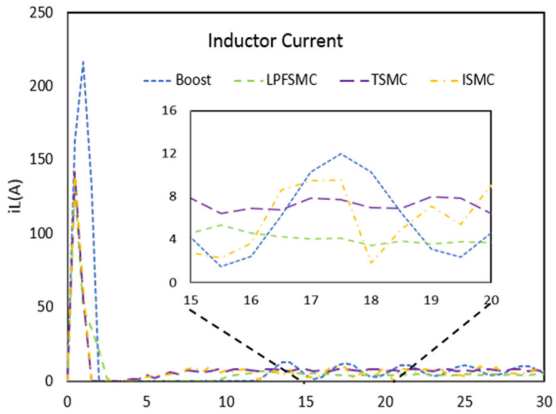

Fig. 6. Inductor current for different control methods.

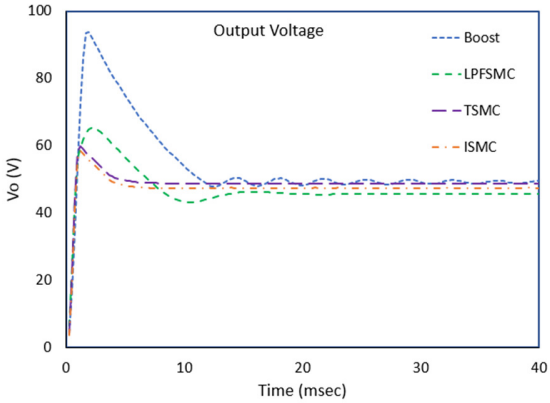

Fig. 7. Output voltage for different control methods.

The simulation results of the output voltage in Figure 7 show that the conventional DC-DC boost converter has a considerable overshoot of up to 91.945 V, t_p = 1.85 ms, t_r = 0.607 ms, t_s = 60 ms, undershoot = 1.884%, and V_o = 49.21 V where the reference output is 48 V. The simulation results of LPFSMC have less overshoot of up to 65.55 V, t_p = 2.3 ms, t_r = 0.495 ms, t_s =12.39 ms, undershoot=1.889%, and V_o=45.59 V. The results of TSMC have the lowest overshoot of up to 60.27 V, t_p =1.13 ms, t_r = 0.474 ms, t_s = 4.9 ms, undershoot = 1.981%, and V_o = 48.72 V. Finally, the results of ISMC have an overshoot of up to 64.28 V, t_p = 1.156 ms, t_r = 0.404 ms, t t_s = 5.27 ms, undershoot=1.887%, and V_o = 48.08 V. These results demonstrate that using slide mode controllers has a better effect on the output response of DC-DC boost converters than using a conventional one. Furthermore, CPL and input variation were tested to validate the stability of the considered SMC methods.

To demonstrate the robustness of different SMCs, the output voltages under a step change of CPL have been monitored. The simulations were carried out for CPL values, of 200 W, 400 W, and 600 W at 0.2 s intervals, corresponding to a second order damping system response. The output voltage attendance of the reference voltage has been considered. The simulations were conducted using a conventional boost DC-DC converter for the case of the CPL in Figure 8. The results demonstrate that the output voltage peak to peak changes within 16.67% of the reference voltage. Moreover, the transient response during the change of the reference voltage had a poor performance.

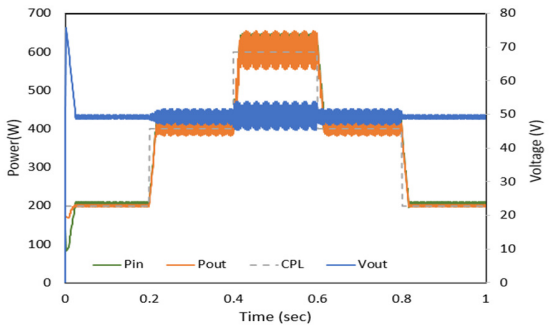

Fig. 8. Output voltage of conventional boost converter with CPL.

The simulation results of LPFSMC are shown in Figure 9. The steady state output voltage is reduced to 45.9 V with a transient response equal to 4.31 V with a percentage change of 9.38%. Figure 10 shows the simulation result of TSMC with CPL. It is worth noting that when the CPL is equal to 200 W, the DC-link output voltage is 50.7 V, when it is 400 W, the DC-link output voltage is 49.44 V, and it is 600 W, the DC-link output voltage is 47.97 V. The TSMC can control the voltage according to the setting of the reference value as required for the steady state response. In Figure 11, it can be seen that the best simulation results are acquired for the ISMC with changing CPL, for transient and steady state performance. TMSC and ISMC improve the DC-link voltage stability with changing CPL. Table II shows the DC-DC boost converter's output voltage and efficiency with variant CPLs for all the considered SMC methods.

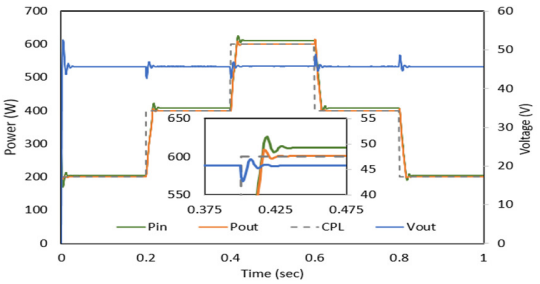

Fig. 9. Output voltage of LPFSMC with CPL.

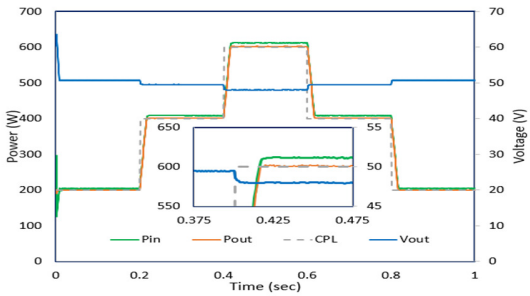

Fig. 10. Output voltage of TSMC with CPL.

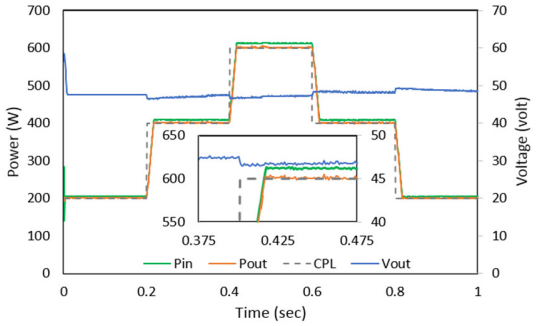

Fig. 11. Output voltage of ISMC with CPL.

TABLE II. DC-DC BOOST CONVERTER OUTPUT VOLTAGE AND EFFICIENCY

	t (s)	CPL (W)	V_{out} (V)	P_{in} (w)	P_o (W)	Eff.
LPF SMC	0.10	200	45.6	204.62	200.08	97.77
	0.30	400	45.73	408.19	400.33	98.08
	0.50	600	45.75	612.04	600.92	98.18
	0.70	400	45.73	408.30	400.38	98.06
	0.90	200	45.66	204.61	200.08	97.78
SMC	0.10	200	50.66	203.94	199.81	97.98
	0.30	400	49.46	408.07	400.32	98.10
	0.50	600	48	611.71	601.09	98.26
	0.70	400	49.48	408.07	400.70	98.19
	0.90	200	50.67	203.95	199.85	97.99
ISMC	0.10	200	47.5	204.55	200.06	97.80
	0.30	400	47.15	407.23	402.44	98.34
	0.50	600	47.21	611.68	601.40	98.32
	0.70	400	48.47	409.90	402.21	98.18
	0.90	200	48.77	203.82	199.88	98.06

IV. CONCLUSION

The conventional CPL has a negative incremental impedance. The instability effect in DC MGs causes negative damping and unacceptably large voltage oscillation when a small variation occurs in the load. This paper proposes a robust slide mode controller to control the DC-DC boost converter feeding constant power load in a DC MG. The simulation results of different slide mode controlling circuits were validated through Matlab/Simulink. The results highlight the robustness and efficiency of ISMC and TSMC. ISMC showed excellent dynamic performance and great stability as it minimized the chattering in output voltage and the settling time as well. On the other hand, LPFSMC showed moderate performance. ISMC could be implemented to provide a significant controlling technique in vast industrial applications.

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