A New Design and Implementation of a Three-Phase Four-Wire Shunt Active Power Filter for Mitigating Harmonic Problems caused by Compact Fluorescent Lamps

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ABSTRACT

The massive embedding of nonlinear loads in industrial, commercial, and residential applications has created severe power quality problems in modern power distribution systems. Compact Fluorescent Lamps (CFLs), which have been designed to replace Incandescent Lamps (ILs), due to their lower energy consumption and longer lifetime, are among the most used non-linear loads. These electric devices, equipped with ballasts and power electronic converters, inject harmonic currents, reactive powers, and create unbalance in the electrical system. Active filters are widely implemented to overcome these issues and improve power quality. In this sense, a Shunt Active Power Filter (SAPF) is developed in this paper to eliminate the under-wanted harmonics caused by multiple CFLs and ameliorate the global power factor in 3-phase 4-wire systems. The suggested SAPF is connected in parallel with the loads and it consists of three main blocks, the reference current calculation block, the Voltage Source Inverter (VSI), and the VSI control block. The reference currents are calculated following the Synchronous Reference Frame (SRF) theory. Meanwhile, Pulse Width Modulation (PWM) based control is adopted for controlling the switching signals. In order to investigate the efficiency and applicability of the developed 3-phase 4-wire SAPF, different simulations and experimental tests are carried out. The measurements are performed by employing a power analyzer and are analyzed with the Power Pad III software. The obtained results disclosed that the proposed SAPF reduced the Total Harmonic Distortion (THD) of the CFL current from 89.6% to 1.62% and improved the power factor.

Keywords-shunt active power filter; power quality; harmonic mitigation; synchronous reference frame theory; hysteresis current controller; pulse width modulation controller

I. INTRODUCTION

Lighting is considered to be one of the most important loads in power networks, accounting for an estimated 25% to 35% of the global generated power [1]. Reducing the total power network load can be achieved by decreasing lighting loads. Compact Fluorescent Lamps (CFLs) are a popular and cost-effective alternative for Incandescent Lamps (ILs) due to their lower energy consumption and longer lifespan. In fact, CFLs consume up to 80% less energy than ILs to produce the same light amount due to their high lighting efficiency [2]. Furthermore, lighting consumers in Tunisia, until 2020, were classified into two categories, those that use CFLs, which represent 77%, where 17% still use classical ILs. Since 2020 and only in new building development, consumers in Tunisia prefer using LED lamps due to their low power consumption, high brightness and efficiency. CFLs function through a chemical reaction, contrasting with ILs that operate based on heating [3]. Each CFL relies on an Electronic Ballast (EB) circuit to create a high frequency output, typically ranging from 10 kHz to 40 kHz. This frequency enables the fluorescent tube to emit visible light due to its internal coating. Basically, the EB in a CFL employs a rectifier to convert the input power, subsequently passed to an inverter that supplies the required ac power to the lamp. Two main ballast types exist for CFLs:

magnetic and electronic [4]. Magnetic Ballasts (MB) employ a coil and core setup to control current, whereas EB rely on solid-state circuits. MBs are the older and bulkier type. They are less energy-efficient and cause visible flickering and humming sounds. On the contrary, EBs are lighter, more energy-efficient, and generate less flickering and noise. They are the favored option for contemporary CFLs. The ballast circuit is mainly responsible for generating harmonics in CFLs, leading to a phase difference between the source voltage and the current, which results in poor power quality and provokes a high harmonic distortion. The latter/These factors can cause disruptive flickering in CFL lamps and create severe issues in the ac line and for the other loads connected at the Point of Common Coupling (PCC) [5]. Thus, a study on the behavior of CFL EBs as well as an accurate modeling of the real lighting system and the application of a suitable compensation are required to overcome those power quality problems. This is vital for adhering to pertinent National and International harmonic standards, such as NTF 15-520 and IEC61000-3-2 [6-7]. These standards are applied for both manufacturers and users, despite the proper compliance in the manufacturing phase. For instance, the General Electric (GE) manufacturing uses a Power Factor Correction (PFC) circuit consisting of an RLC branch before the ac-dc converter, and electromagnetic interference (EMI) filters after the rectifier to maintain the THD within the imposed limits. Unfortunately, the massive use on the users' side for example in residential, commercial, or industrial applications can cause in a certain case the noncompliance with the standard limits [8]. Therefore, several solutions have been proposed in the literature to maintain the Total Harmonic Distortion (THD) of the massive use of non-linear loads, such as Passive Filters (PFs), within limits. However, despite their advantages, PFs have some limitations, including limited effectiveness in transient conditions, presence of higher order harmonics, and resonance issues. Additionally, PFs have fixed compensation characteristics and a large physical size [9-10]. To address these limitations, researchers have developed new power electronic interfacing devices called Active Power Filters (APFs), which are designed for reactive power and harmonic compensations, and can effectively overcome the drawbacks of PFs. Generally, the APF devices are connected at the PCC in series or in parallel with the power system [11]. Among multiple options, the compensation methods using series converters are considered to be a cost-effective solution [12] compared to the back-to-back (B2B) converters [13] or the Unified Power Flow Controllers (UPFCs) [14]. However, parallel APFs called Shunt (SAPFs) remain the most widely adopted method/solution due to their compensation flexibility, which is performed by controlling the current injection. SPAFs detect harmonics and reactive power in the electrical system and generate cancellation currents to compensate them, reduce the THD, increase power factor, and stabilize the electrical system [15]. SAPFs operate as a power source equipped with a Voltage Source Inverter (VSI) situated at the PCC alongside the power network. Its role is to counterbalance the harmonic currents produced by the nonlinear load. Generally, a SAPF consists of three main blocks: the power device block, the reference current calculation block, and the power switches control block. From the literature review, it is found that several typologies of SAPF filters have been invented during the last years [16-17].

In this study, a SAPF based on a three legs with a middle point 2C capacitor VSI topology is developed. The main role of this filter is to reduce the harmonics generated by nonlinear loads. The proposed SAPF can also perform other tasks, such as making the current an active component. The SAPF is connected in parallel at the PCC with a 3-phase 4-wire nonlinear load consisting of new GE model of CFLs distributed over 3 AC phases. The fourth wire of the electrical power system (the neutral) is connected in the middle of the two capacitors. The new studied model, which consists of a 20W GE CFL and is extracted from the EB of the lamp, presents the first original goal for this paper. Many experimental and simulation modeling tests were carried out to investigate the model. The results show high closeness between the real and the simulation findings, in terms of source current and voltage waveforms. Also, the found THD of the GE CFL is around 90%, and the CFLs current waveforms are non-sinusoidal.

In the light of the preceding discussion, it can be inferred that the operating efficiency of the SAPF is based on the effectiveness of the reference current extraction technique and the VSI control switching devices block. For the reference current extraction, a mathematical algorithm based on the SRF technique is developed and implemented [18], in order to extract in real time the harmonics generated by the CFLs to the power source. Those currents are sensed using four sensors placed in the load side. The SRF technique also deploys a PLL block to provide the fundamental frequency for synchronization. Meanwhile, the compensation currents are compared to the actual currents offered by the VSI at the PCC. The current errors given by the comparator are applied to the HCA to provide the switches signal control for the VSI based IGBT switches. While the HCA has numerous advantages [19], it is worth noting that the issue of chattering, which can result in variable switching frequencies, remains unresolved. To address this concern, a PWM controller is integrated into the system instead of the HCA [20], to stabilize the switching frequency and mitigate the associated harmonic losses. From the simulation results, it is observed that the SAPF with SRF and PWM greatly improved the power quality of the source current and reduced the harmonics generated by GE CFLs to 1.62% instead of 90%. Moreover, the use of PWM controller instead of the HCA achieved a constant and controllable switching frequency, which is not possible with the HCA.

II. DESCRIPTION OF THE STUDIED CFL

A. Experimental Setup for One CFL

The most popular original brands of CFLs in Tunisia are Philips, GE, and Osram. In this study, the GE type is adopted due to its availability in the laboratory. This device is the GE FLE-20-W-230V, 50Hz, 120mA, 1152 Lim, 6500 K and it is made in China. The studied CFL, also called compact fluorescent light, energy-saving light, and compact fluorescent tube, is a fluorescent lamp designed to replace an IL. The CFL circuit has been designed for a nominal mains voltage of 230 V_{rms}, 50/60Hz. The mains voltage operating range is between 200 and 250 V_{rms}. Figure 1 depicts in detail the main

components of the studied lamp. Figure 1(a) presents the overall model of the lamp, whereas Figure 1(b) and Figure 1(c), present the upper and lower side view of the EB of the lamp, respectively. The main concern of the widespread use of CFLs regards the power quality problem. To quantify this problem and then overcome it, some studies regarding CFL modeling have been developed [21-22]. Considering the different existing methods of CFL modeling, this study deliberately chose a simplified model called current model according to its availability in the laboratory. The latter was used in previous research [23] to study the practical effect of some harmonics of a low voltage generator source on the main network. Unfortunately, the authors did not present the load model, which is one of the main objectives of the current manuscript. To develop this model, an experimental measurement for a single CFL as observed in Figure 1(d) is conducted to survey the amplitude and phase angle of each current harmonic.

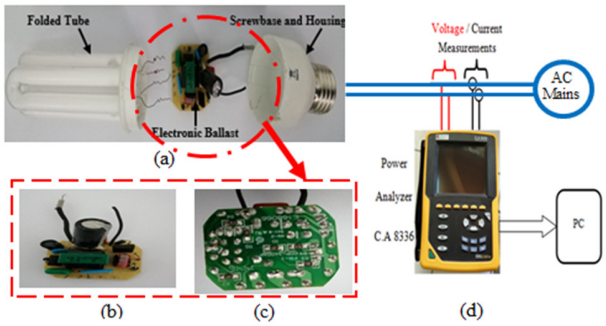

Fig. 1. Components of the 20-W and experimental setup for one GE CFL. (a) Open full model of GE lamp, (b) upper side, (c) lower side, (d) experimental setup.

As noticed in Figure 1(d), the Chauvin Arnoux C.A 8336 power analyzer is put into service to obtain the values of the electrical parameters. This device is used to visualize data on the spot and store them in a digital form, which can be retrieved later. All the experimental figures of this section come from the software proposed by the manufacturing companies (the latest version) called Power Pad III [24]. The device employs (1) to calculate the different harmonics (X_{THD}) for both the voltage and the current. Moreover, the corresponding angle (φ_k) with respect to the fundamental in degrees (°) can be calculated using (2). It should be noted that the computations were performed using a 16-bit FFT with 1024 data points spanning 4 cycles and utilizing a rectangular window as specified in IEC61000-4-7. From the real parts (b_k) and imaginary parts (a_k) expressed by (3), the harmonic factor is calculated for each phase (j) and for each order (h) [25].

$$X_{THD}[j] = \frac{\sqrt{\sum_{h=2}^{50} X[j][h]^2}}{X[j][1]} \quad (1)$$

$$\varphi_k = \arctan\left(\frac{a_k}{b_k}\right) - \varphi_4 \quad (2)$$

$$\begin{cases} a_k = \frac{1}{512}\sum_{S=0}^{1024} F_s \cos\left(\frac{k\pi}{512}s + \varphi_k\right) \\ b_k = \frac{1}{512}\sum_{S=0}^{1024} F_s \sin\left(\frac{k\pi}{512}s + \varphi_k\right) \end{cases} \quad (3)$$

where X represents the signal measured by the device, which can be the current or the voltage of the load. $X[j]$ [1] represents the fundamental signal for each phase j ($1 \leq j \leq 3$), h represents the harmonic index, Fs is the sampled signal at the fundamental frequency f_4, and k is the index of the spectral spike. Note that the order of the harmonic component is equal to $k/4$.

The main parameters measured for the line source are the true RMS voltage, the true RMS current A_{rms}, the active power P (W), the reactive power Q (VAR), the apparent power S (VAR), the frequency F (Hz), the power factor PF, the THD voltage (V_{THD}), and the THD current (I_{THD}) as percentages. Peak voltage, the peak current and the phase of harmonics for voltages and currents up to the 50th order are measured. Figure 2(a) illustrates the measured voltage and current waveforms absorbed by one CFL model. Figure 2(b) displays the CFL current harmonic spectrum up to the 50th rank. Table I summarizes the RMS values of power quantities, representing the fundamental, harmonics currents, and the phase angle between the CFL current and the voltage.

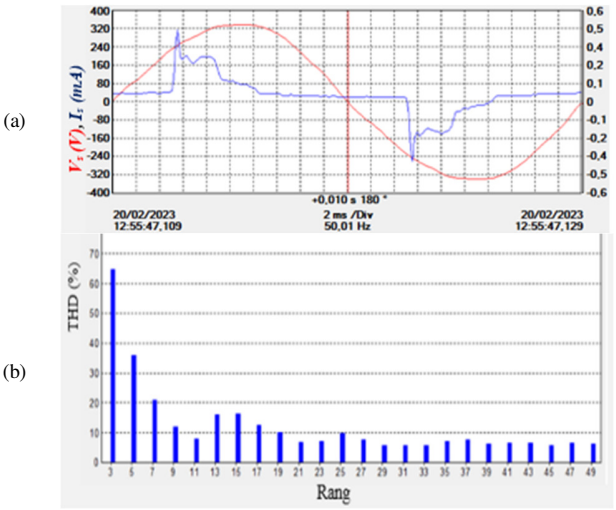

Fig. 2. (a) Experimental current and voltage waveforms provided by the power analyzer for one CFL. (b) Experimental current spectrum of one CFL.

TABLE I. SUMMARY OF THE EXPERIMENTAL MAIN PARAMETERS MEASURED FOR THE LINE SOURCE OF ONE CFL PROVIDED BY THE POWER ANALYZER.

A_{RMS}	V_{RMS}	P	Q	DPF (cos(φ))
0.16 mA	241.9 V	22.36 W	30.7 VAR	0.928
F	PF	A_{THD}	V_{THD}	φ (°)
50 Hz	0.641	87%	4.6%	22°

During the experimental test phase, the GE lamp was supplied by a $V_{\_RMS}$ =*241.9* V-50 Hz line. From Figure 3, the current curve is non-sinusoidal, and phase-delayed to the voltage with φ =22° (as presented in Table I), which implies partial network distortion. From Figure 2 and Table I, the total distortion rate is A_{THD} = 87% related to the fundamental with a poor PF equal to 0.641 and a high value of reactive power equal to 30.7 VAR, which is remarkable despite the low real power (21.46 W).

B. Experimental Results for a Large Number of CFLs in 3-line Source

To measure the effect of a large number of CFLs on the distribution network, a test bench was produced in the laboratory. This bench contains 75 lamps distributed over 3 AC phases (25 lamps in parallel for each phase). It should be noted that the same experimental measurement procedure carried out for a single lamp (as presented in Figure 1(d)) was applied for this new arrangement. The test was conducted using the same C.A 3 analyzer, which was now configured in 3-phase 5-wire mode (a, b, c, neutral, and Ground). From the previous founded result in Figure 10 [27], it is easy to see that the CFLs currents waveforms are not sinusoidal for the three phases, and the neutral current is not equal to zero. The results indicate an increase in voltage V_{THD} from 3.4% to 5.3%. This value is outside the order of National and international standards [6, 7, 28, 29]. The A_{THD} values for the three phases are 86.2%, 88.5%, and 90.4%. From Table I, it can be also seen that the CFLs current was delayed to the voltage with 22° for the three phases, which may have harmful effects on the distribution network. In order to investigate more the behavior, and in order to ameliorate the power quality and to compensate the decided reactive power Q, it is necessary to move up from the testing phase to the simulation phase (modeling phase), which is the purpose of the next section.

C. Simulation Model of the Studied Lamps with PSIM

To achieve the objective mentioned above, the EB appearing in Figure 1 of the studied lamp is modeled using the PSIM software, as manifested in Figure 3. This model is identified from the EB of the lamp where the tube of the lamp is modeled by an equivalent resistance R_{ch} equal to 100 Ω [21-22]. The GE manufacturing line uses an RLC filter consisting of *R1*, *L1* and *C2* on the main side and a PFC in the DC side in order to reduce the passage of the harmonics to the network and to comply with the standards' limits.

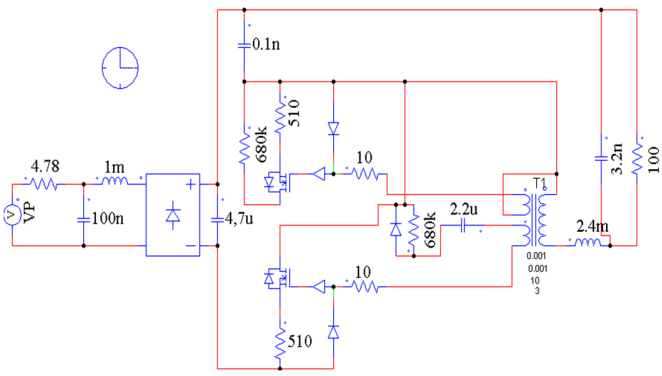

Fig. 3. Simulation model of 20W GE CFL lamp with PSIM.

D. Simulation of the Equivalent Model of one CFL Lamp

Technically, a traditional lamp of residential use, with a power lower than 30W, is equipped with an EB composed of four blocks. However, for economic reasons (valid only in simulation), such a lamp can be represented by an equivalent model composed of a simple rectifier with a capacitive filter in parallel at its output, and an equivalent resistive load [26]. Yet, this model includes at its input an RLC filter, connected in series with the rectifier bridge as presented in Figure 4. The rectifier circuit then supplies power to a load represented by the resistance and in an attempt to minimize the ripple effect in the load resistance, a capacitance *C2* is introduced. The interplay between these three blocks, defines the circuit's dynamics and shapes the current waveform drawn by the circuit. Figure 5 exhibits the equivalent model of a GE lamp tested in the laboratory such that the circuit is supplied by a 230 V - 50 Hz alternating voltage source. Figure 5(a) represents the curve of the current absorbed by this non-linear load of the equivalent model as well as of the real model of the studied lamp, and Figure 5(b) shows their Fast Fourier Transform (FFT) components. According to [3], several tests were performed to determine the approximation of the value of the equivalent resistance (R_{eq}). In this study the specific value is found around 2400 Ω. It should be noted that a small MATLAB (.m file) algorithm was developed to depict the results generated by CFLs, representing both the experimental current waveforms from the CA.8336 analyzer and the simulated current waveforms from the PSIM software in the same Figure (Figure 5).

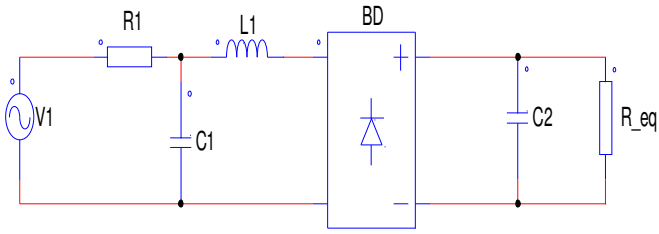

Fig. 4. Simulation equivalent model of one CFL lamp in PSIM Software.

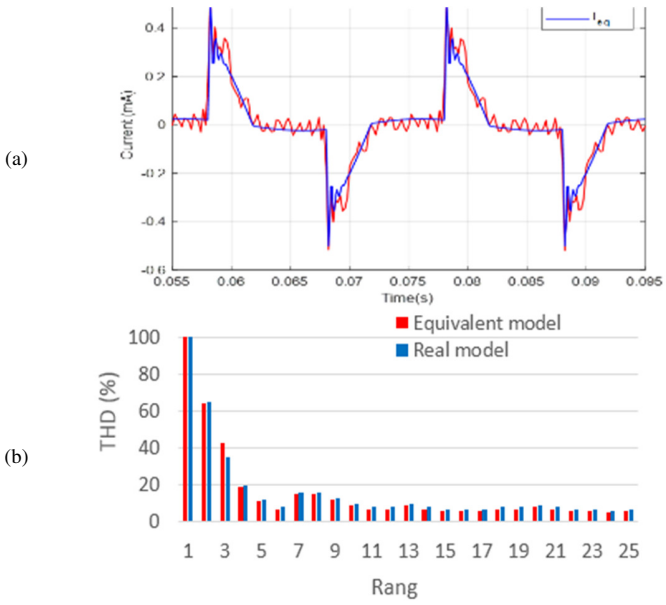

Fig. 5. (a) Simulation and experimental current of the real model and the equivalent model waveforms for one CFL. (b) Their current FFT components.

The simulation results of the studied equivalent model of one GE CFL presented in Figure 5(a) and Figure 5(b) disclose

that this model has the same amplitudes and shape characteristics with the real model. In addition, the same effects generated by the real model on the network are noticed in the equivalent model. Thus, this equivalent model can be used for simulation purposes. In order to improve the power quality and to cancel the harmonics generated by the non-linear loads on the mains side, an active power filter for harmonic and reactive currents compensation applied for the same equivalent model will be presented below.

III. SYSTEM CONFIGURATION AND MODELING OF THE SAPF

The power circuit of the system is composed of three main parts. The first part includes the power network source, which is a balanced 3-phase power supply designed with $Vs_{(a,b,c)} = 380$ V, 50 Hz. The second part is the non-linear load, consisting of 75 lamp models distributed over the 3-AC phases, 25 lamps in parallel for each phase. The last part is the VSI placed at the PCC in parallel with the power network. This VSI acts like a power source to compensate the harmonic currents generated by the non-linear load. Therefore, for the rest of this paper, the grid voltage $Vs_{(a,b,c)}$, the load, and the APF currents $I_{L_{(a,b,c)}}$, $I_{f_{(a,b,c)}}$, are the sensing requirements. The control part of this system is developed based on the SRF Theory, which will be explained in the following section. The VSI switches $F_{(a,b,c)}$ are controlled with a simple hysteresis controller by comparing the compensating current $I_{C_{(a,b,c)}}*$ to the reference current $I_{r_{(a,b,c)}}$. The controller will be also discussed in detail in the following section. The SAPF construction is crucial for precise compensation, and the controller must meet specific requirements, including managing and providing harmonics currents, controlling reactive power with fundamental frequency components, and maintaining continuous DC voltage across the energy storage element. To verify the power and control performance, the inverter can be assumed to feed a sinusoidal voltage source corresponding to the connected load. The SAPF controller can then control the reactive power and reduce the harmonics caused by the non-linear loads, with filter performance analyzed to generate compensation currents. The full system bloc diagram containing the power circuit and the control circuit is presented in the Figure 6.

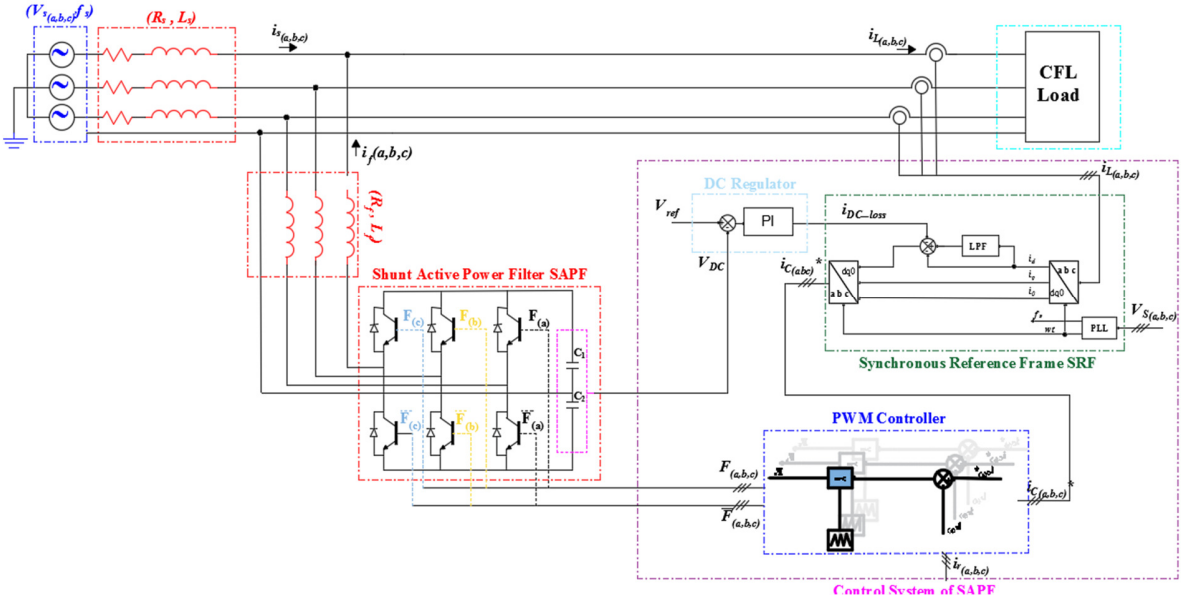

Fig. 6. The circuit diagram of the 3-phase 4-wire SAPF with SRF and PWM control.

A. *Conventional Hysteresis Band*

The conventional fixed-band hysteresis consists of two bands called the upper band (Δ+) and the lower band (Δ-). The modulated (switching) current is trapped between those bands. So, when the error current ε_a tries to touch the upper band Δ+, the upper IGBT switch F_a is turned off and the lower switch $\overline{F_a}$ is turned on. The behavior is similar for the lower band Δ-. This causes the compensating current $I_{C_{(a,b,c)}}*$ to follow the reference current $I_{r_{(a,b,c)}}$. This method is used due to its robustness and good dynamic performance, which are not possible with other types of compensation. Figures 7(a) and 7(b) display the block diagram of the conventional hysteresis control and its signals waveforms for only a single phase (phase *a*). It should be noted that the same procedure is carried out for the other phases (phases b and c) to obtain the control signal $F_{(a,b,c)}$ for the high side of the three-phase inverter. The lower side of the inverter $\overline{F_{(a,b,c)}}$ is controlled by the same, but inverted, output signal.

B. *Pulse Width Modulation Current Control Technique*

The PWM technique is commonly utilized in SAPF to control the current and counteract the negative effects caused by nonlinear loads in the power system. By generating a switching signal that adjusts the duty cycle of a power electronic switch, such as a transistor or a MOSFET, the filter can regulate the amount of the current injected into the system and eliminate the harmonics and reactive power. The benefits of using this technique include high efficiency, low harmonic

distortion, and accurate current control [30]. However, the implementation of the PWM technique requires a sophisticated control algorithm to generate the switching signal and modify the duty cycle in real-time. Overall, the PWM current control technique is an efficient solution to improve power quality and mitigate the issues associated with nonlinear loads in the power system. Figure 7(c) shows the block diagram of the PWM control technique. Like the conventional hysteresis control, this control generates the difference between the reference current $I_{C_{(a,b,c)}}$ * and the actual current $I_{r_{(a,b,c)}}$. Then the error is applied to the input of a regulator. The output signal of the controller, called modulator, will be compared to a triangular signal of a fixed frequency, called carrier, in order to determine the switch orders of switches $F_{(a,b,c)}$. The carrier signal has a fixed frequency, so the cutting frequency of the power semiconductors is also fixed.

IV. VALIDATION OF THE PROPOSED TECHNIQUE USING NUMERICAL SIMULATIONS

With the aim to test the proposed technique for the compensation issue of the reactive power and the harmonic currents injected by the CFLs on the Power Network, circuit diagrams of both methods with the conventional hysteresis control bloc and with the PWM control bloc (Figure 6) are designed and simulated. Table II summarizes the full details of the proposed parameters for the load, power system, and SAPF parameters used in this study. For the rest of this paper, it should be noted that the non-linear load is connected to the power supply at *t=0s*, whereas the SAPF is enabled at *t=0.02s*. All parameters are measured after connecting the SAPF for both hysteresis control and PWM control techniques.

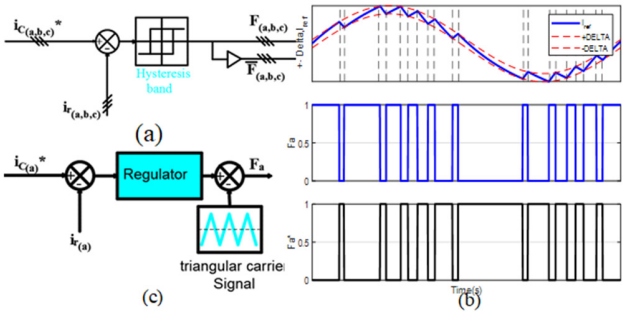

Fig. 7. a) Block diagram of the constant hysteresis modulation. (b) Hysteresis band current control in switches F_a and F_a*. (c) Block diagram of the PWM current control technique.

TABLE II. POWER SYSTEM PARAMETERS

Parameters		Symbol	Values
Grid	**System frequency**	F_s	50 HZ
	Source voltage	V_{rms}	230 V
	Source resistance	R_s	mΩ
	Source inductance	L_s	µH
Non-linear load	**Load capacitance**	*C1, C2*	100 nF, 4.7 µF
	Load inductance	*L1*	1 mH
	Load resistance	*R1* and R_{eq}	4.7 Ω,2477 Ω
Shunt active power filter SAPF	**Filter resistance**	R_f	1 mΩ
	Filter inductance	L_f	0.1 µH
	Dc side capacitance	C_f	2200 µF
	Reference voltage	V_{dc}	600 V

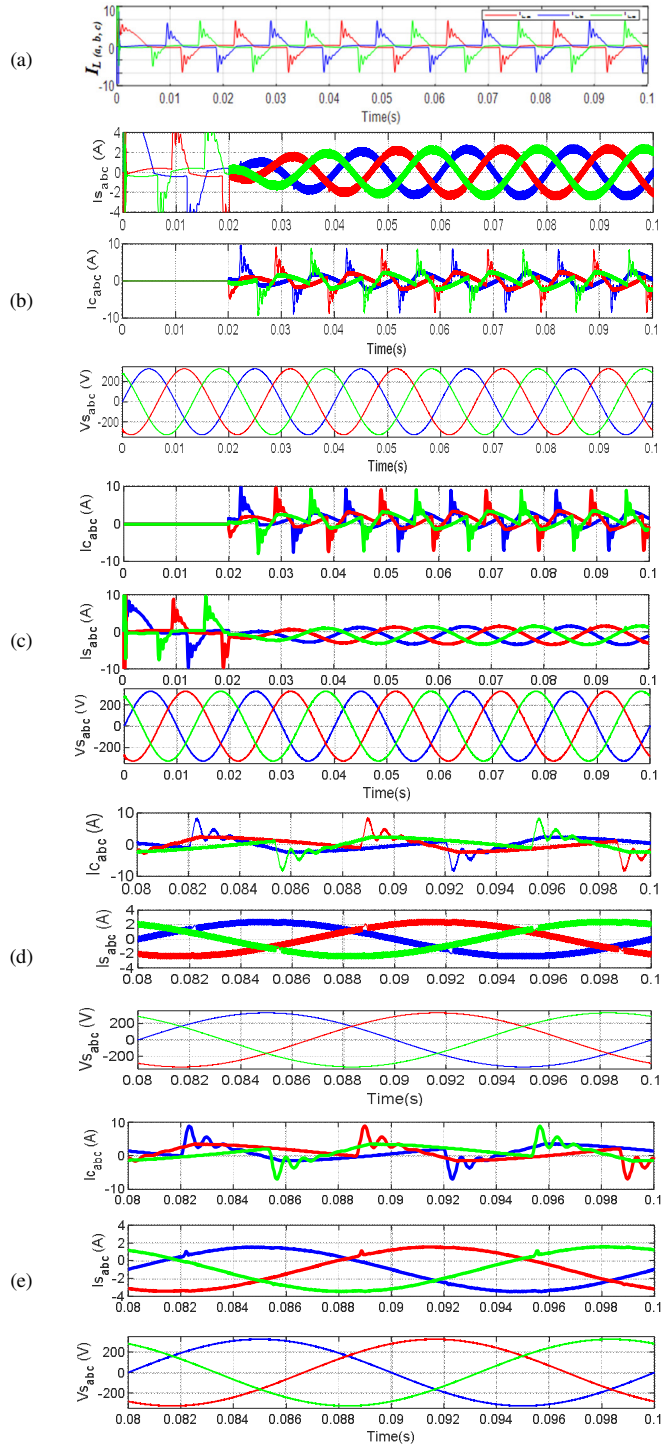

Fig. 8. Simulation circuit currents waveforms at different points of SAPF before and after compensation: (a) Load currents before compensation, (b) with the hysteresis controller, (c) with the PWM controller, (d) and (e) X currents of (b) and (c) but with a zoomed scope from t=0.08 s.

$I_{L_{(a,b,c)}}$, $I_{C_{(a,b,c)}}$, $I_{S_{(a,b,c)}}$ and $V_{S_{(a,b,c)}}$ are the load currents before compensation, the compensating current injected by the

power device (the SAPF), the source currents after compensation, and the source voltage, respectively.

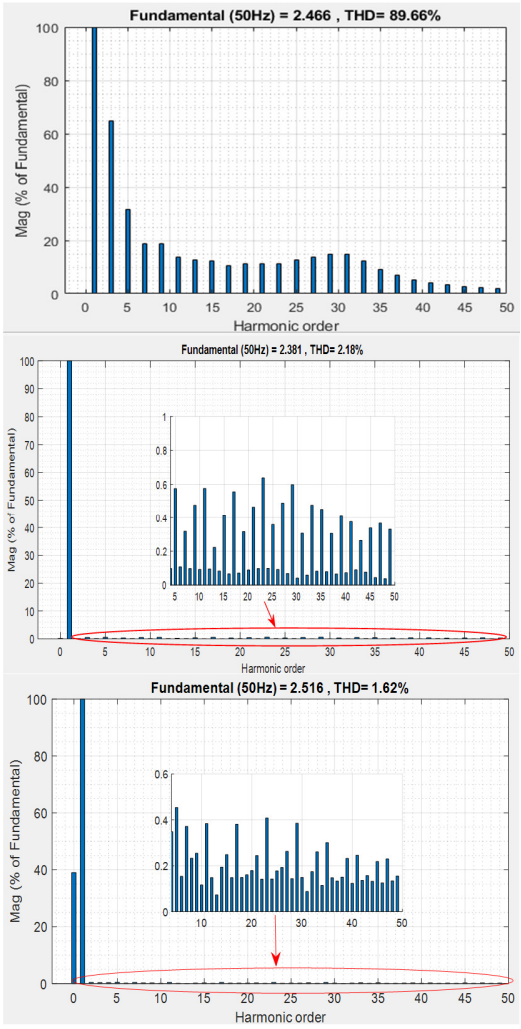

Fig. 9. Simulation FFT components of the source currents (a) before compensation and after compensation (b) with the hysteresis controller and (c) with the PWM controller.

A. *Performance of the Conventional Technique*

As observed in Figures 8(a), 8(d), and 9(a) that represent the FFT component and the current waveforms of the CFLs before connecting the SAPF, the THD of the current A_{THD} = 90.4%, and the THD of the voltage V_{THD} = 5.3%. Moreover, the same Figures indicate that the system corresponds to a poor factor due to the phase shift between the current and the voltage. According to the national [6-7] and the international [28-29] standards, these results are outside the allowed limits and can cause harmful effects on the distribution network. As a consequence of this work and after connecting the SAPF at t = 0.02 s to the system, it is clear from Figures 8(b) and 8(e) that the currents waveforms of the source $I_{S_{(a,b,c)}}$, become almost sinusoidal, which attests that the conventional algorithm used in this paper succeeded in compensating the harmonic currents by injecting equal but opposite harmonic currents to the power network. In addition, the source currents and voltage are in phase, which results in obtaining a good PF close to 1. Figure 9(b) reveals that the THD of the current A_{THD} after compensation becomes equal to 2.18%. A good reduction in THD is noticed and the fundamental current values for phase a remain almost the same before and after connecting the APF to the system, where $I_{S\_Bef\_1a}$ =2.466 A and $I_{S\_Aft\_1a}$ = 2.388 A. This implies that the filter injects only harmonic currents, whereas the network injects only the fundamental component of the load current.

B. *Performance of the PWM Control Technique*

The currents waveforms simulation results for the SAPF before and after compensation with the PWM controller have already been presented in Figures 8(a), 8(c), and 8(e). Figures 10(a) and 10(b) represent the same results for the single phase a. To further investigate the proposed PWM technique, the error signals for both fixed-band hysteresis and PWM band are also investigated. In this case, it can be noticed that the use of the PWM control technique on the system instead of the fixed-band hysteresis $\Delta(t)$ can improve the quality of the source current waveforms $I_{S_{(a,b,c)}}$. This leads to an amelioration in the power factor and a reduction in the THD A_{THD} = 1.62%, as depicted in Figure 9(c), instead of A_{THD} = 2.18% produced by the conventional hysteresis controller. This results in better filtering performance, achieving the lowest THD value. Referring to the international standard, the results are in accordance and follow very well the limits.

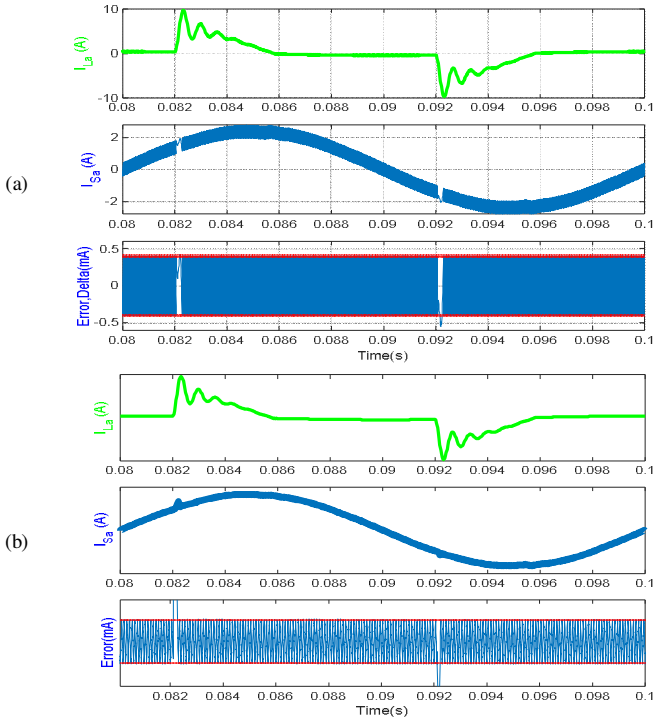

Fig. 10. Simulation error signal and source currents waveforms before and after compensation for hase a controlled with: (a) the hysteresis controller and (b) the PWM controller.

V. FUTURE RESEARCH

The SAPF presented in this manuscript, is designed to compensate high harmonics, reactive power, and other disturbances caused by only CFLs loads (THD > 90%), thereby improving the power factor and overall system performance, which has not been achieved in previous research. Past studies focused only on 3-phase rectifier connected to RL loads, which inject (THD<35%), or on CFL with linear loads (THD <50%). This load represents a big challenge for the Tunisian power system. At the same time, the applicability and effectiveness of the suggested SAPF were tested and evaluated. However, despite all the advantages of the SAPF, the DC bus of this filter uses a 3-phase rectifier to provide the power energy to the two middle point capacitors to compensate the reactive power generated by the nonlinear loads, which can create more problems of harmonics in highly non-linear loads. To overcome this issue, a Hybrid Active Power Filter (HAPF) combining shunt and series active power filters can be suggested for future work. SAPF can be applied in parallel with wind systems [31]. Also, with the current trend of Artificial Intelligence (Neural Networks, Fuzzy Logic, Evolutionary Computing), the HAPF will be simulated and investigated with new control algorithms to enhance SRF and PWM control capability. The full new system can be be applied for LED lamps, which represent a future new challenge in Tunisia and in the global world power system. Moreover, the full systems must be investigated under some other load conditions (e.g. charger drivers, TVs, etc.) and under different scenarios, including balanced and unbalanced nonlinear loads

VI. CONCLUSIONS

A new GE model and equivalent model of 20 W Compact Fluorescent Lamp (CFL) was developed and implemented based on many experimental and simulation tests. This model is extracted directly from the Electronic Ballast (EB) of the lamps, which is the first main achievement of this paper. This type of load injects high harmonics to the main system, something that is affirmed by the experimental results. Hence, a 3ph-4W SAPF with a middle-point capacitor topology, connected in parallel with this high nonlinear CFL loads is proposed. This filter is able to solve harmonic and reactive power compensation issues caused by the nonlinear behavior of CFLs. This filter comprises three legs based on two stages and with a capacitor midpoint topology, where the network is connected in parallel with the three legs of the IGBT power switches and the fourth wire, representing the neutral, is connected to the middle of the two capacitors. The SRF theory is adopted to generate the reference currents for the controller. The VSI, which is the core of the SAPF, is controlled by an HCA and a PWM control technique. The PWM controller is used to generate the gate pulses necessary for the VSI. Simulation and experimental results demonstrated the effectiveness and successful performance of the proposed SAPF in mitigating those high harmonics injected by the load, improving the power factor, and in compensating the decided reactive power, which nowadays represents a real challenge in power systems.

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