DC-38GHz Nonuniform Distributed Amplifier Design with Gate and Drain Line Optimization Using 0.1µm GaAs pHEMT Technology

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Received: 18 March 2023 | Revised: 4 April 2023 | Accepted: 5 April 2023

 DOI: https://doi.org/10.48084/etasr.5859

ABSTRACT

This paper presents an optimized three-cell Nonuniform Distributed Amplifier (NUDA) suitable for optoelectronic drivers in the Q band. This is the first NUDA of Darlington topology designed with the 0.1µm GaAs pHEMT process with a transition frequency f_T of 130GHz. Gate microstrip line sections, drain microstrip line sections, and active device sizes were optimized to obtain high gain and large bandwidth from a Monolithic Microwave Integrated Circuit (MMIC) Distributed Amplifier (DA). This paper presents two NUDA designs with different topologies. The first was designed with a three-stage Common Source (CS) topology that enhanced the bandwidth up to 34GHz with a gain greater than 8dB, and the second was designed with two Darlington stages and one CS stage that enhanced the bandwidth up to 38GHz with a gain greater than 8dB. The bandwidth enhancement of NUDA with the Darlington topology was compared and verified with the NUDA of common source topologies.

Keywords-Monolithic Microwave Integrated Circuit (MMIC); Distributed Amplifier (DA); pseudomorphic High Electron Mobility Transistor (pHEMT); Gallium Arsenide (GaAs); optimization; Nonuniform Distributed Amplifier (NUDA)

I. INTRODUCTION

The demand for wideband applications in the crowded lower K and Ka bands has forced designers to choose the Q band for modern wideband designs. Distributed Amplifier (DA) design is the best choice for wide bandwidth applications like optical drivers [1]. DAs were designed at first with vacuum tube technology. Later on, MMIC DAs were designed with the MESFET technology. With high electron mobility and high transition frequency features of GaAs, InP HEMT technologies dominated the DA designs in the 90s. The first DA designs were uniform in nature and all gate and drain transmission line sections had the same inductance values [2]. Later, using optimization, nonuniform distributed amplifiers were implemented by varying the parameters of the distributed amplifiers [3]. The common source [4-5] and cascode [6-8] topologies are the most commonly used in DA design. In [5], a uniform DA design used a gain control switch and 8 GaN HEMT cells of CS topology to obtain 8±1.5dB gain. As cascode topologies are very sensitive, they need an extra stability network. In [6], a 5-cell cascode topology DA with a stability network obtained a gain of 11.23dB and a bandwidth of 10MHz-22GHz. In [7], a 6-cell cascode DA topology with dual gate device mode obtained a DC-33GHz bandwidth with a gain of 10.6dB. Another 6 cell cascode DA topology [8] with a series R and C network at the device gate obtained a DC-40GHz bandwidth with a gain of 12dB. However, the first proposed DA design with CS topology without any additional network obtained competitive gain and bandwidth with the minimal number of 3 cells only. The proposed design also offers the highest transition frequency (f_T). The second proposed DA design used the Darlington topology [9] to enhance bandwidth. The Darlington triplet offers 3 times the transition frequency f_T of a single HEMT and handles high current and high frequencies. The high transition frequency plays a significant role in improving the bandwidth of DA. In both proposed designs, nonuniform design using gate optimization and drain microstrip lines were carried out with GaAs pHEMT technology, where all gate and drain microstrip line sections had different inductance values. This design drives the perception of NUDA using GaAs pHEMT in mm-wave applications [10-12]. Proper selection of the active device, gate and drain line optimization, and active device size balance the tradeoff between gain and bandwidth. The pp1010 GaAs pHEMT was selected as the active device for this design. Simulations of this design were carried out with a 100nm gate length GaAs pHEMT technology on 2mil (50µm) substrate thickness to achieve high gain. The high transition frequency f_T of 130GHz and the optimized size of the active device had significant contributions in achieving high bandwidth and gain.

II. 0.1µm GAAS pHEMT MMIC TECHNOLOGY

The pp1010 GaAs pHEMT used in the DA design has a gate length of 0.1µm generated using the E-beam process with a substrate thickness of 2mil. The T-gates are generated using the electron-beam lithographic process. The InGaAs channel has a pinch-off voltage of -0.95V at I_D=1mA/mm and can be operated up to a maximum drain bias of 4V. The device is passivated using nitride and can be used as a dielectric for 400pF/mm^2 Metal Insulator Metal (MIM) capacitors. These passive components support the MMIC fabrication process. Two thick metals with an air bridge are used as interconnection. The highest transconductance (g_m) of the device is 725mS/mm at V_{DS}=1.5V and the maximum drain current I_D is 760mA/mm at V_{GS}=−0.5V. At peak transconductance, V_{GS} is −0.28V. The device has a maximum gate-to-drain breakdown voltage of 9.6V. The device's maximum oscillation frequency ($f_{\max}$) is 180GHz at V_{DS}=1.5V. The device's transition frequency is 130GHz at V_{DS}=1.5V. Table I shows all the features of the 0.1µm GaAs pHEMT.

TABLE I. FEATURES OF THE 0.1µM GAAS pHEMT

	Feature	value
1	Gate length	0.1µm
2	Pinch off voltage	-0.95V
3	Breakdown VDG	9.6V
4	IDSS	520mA/mm
5	Maximum gm	725mS/mm
6	IDmax	760mA/mm
7	fT	130GHz
8	fmax	180GHz
9	MIM capacitor	400pF/mm
10	TFR resistor	50ohm/square
11	Epi resistor	135ohm/square

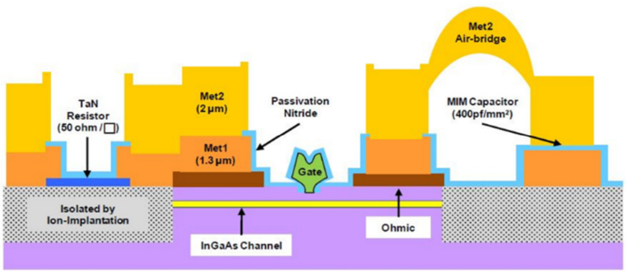

Fig. 1. Cross section of the pp1010 GaAs pHEMT.

III. CIRCUIT AND DESIGN

A. 3-Cell NUDA Design with CS Topology

Figure 2 shows a simplified schematic of the 3-cell NUDA with CS topology. Each cell was implemented with the WIN semiconductor pp1010 pHEMT process on 0.1µm GaAs substrate. All cells were connected in a CS configuration. All gates were connected with microstrip lines. Similarly, the drains were interconnected with microstrip lines from one cell to another. Supplied with a gate bias of -0.35V, provided a drain bias of 1V and a quiescent drain current I_{DSS} of 63.9mA.

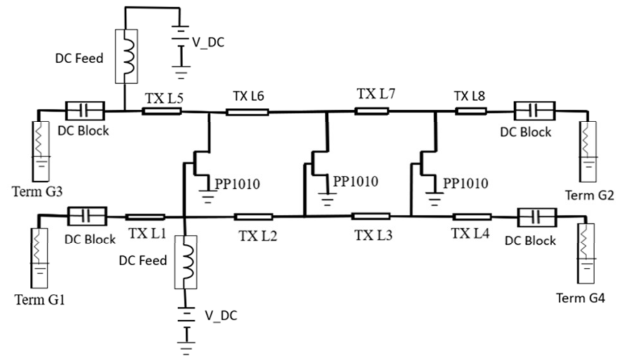

Fig. 2. Cell architecture of the distributed amplifier.

As the number of cascaded cells increases, the gain should increase, but this is not the case for the DA because as the number of cells increases, the voltage wave gets more attenuated as it travels through the transmission line and the gain reduces. Therefore, the optimum of 4 cells [13] were needed in this design to achieve a greater than 8dB gain. The optimized lengths of the gate transmission line sections were TX L1=100.053µm, TX L2=327.455µm, TX L3=147.222µm, TX L4=537.156µm and the optimized lengths of drain transmission line sections were TX L5=533.489µm, TX L6=255.256µm, TX L7=1036.54µm, and TX L8=912.267µm. In addition to optimizing drain and gate transmission lines, the proper selection of device size plays a vital role in achieving a high gain. The gain was reduced for device sizes larger than 4×50µm. Similarly, the optimal bias of V_{GS}=-0.5V and V_{DS}=1.5V is needed to achieve a better tradeoff between gain and bandwidth. The amplifier design was perceptively optimized to achieve optimal performance while maintaining the required gain and bandwidth.

B. 3-Cell NUDA Design with Darlington Topology

In order to enhance bandwidth, the first and second cells used the triple Darlington topology and the third cell used the CS topology, as shown in Figure 3. The triple Darlington topology offers 3 times the transition frequency (f_T) of a single transistor [14].

$$w_{T,D} \cong 3.05\, w_T \tag{1}$$

Therefore, it handles high current and high gain at higher frequencies, compared to the CS stage, is very popular for broadband amplifiers, and extends bandwidth to microwave frequencies. The optimal sizes of M1 and M2 were 4×50µm and 4×25µm for M3. In the triple Darlington topology, the condition W1,W2=2W3, provides a wide bandwidth compared to other width choices for HEMTs. The optimized lengths of the gate transmission line sections were TX L1=80µm, TX L2=261.826µm, TX L3=117.716µm, and TX L4=531.156µm, while the optimized lengths of drain transmission line sections were TX L5=426.246µm, TX L6=203.944µm, TX L7=828.174µm, and TX L8=728.882µm. A better tradeoff between gain and bandwidth was obtained at biasing values of V_{GS}=-0.35V and V_{DS}=5V.

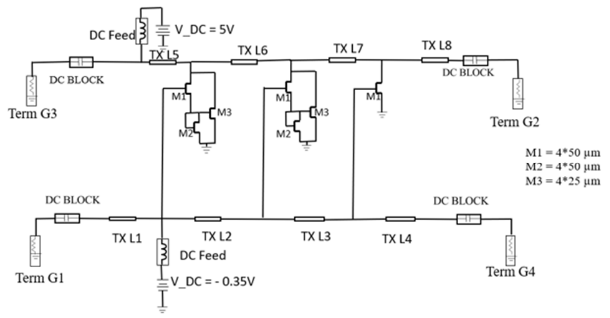

Fig. 3. Cell architecture of the Distributed Amplifier.

IV. RESULTS AND DISCUSSION

The inductive lengths of the gate and drain were adjusted iteratively until a maximum gain of 11dB was achieved. Figures 4-6 show the simulated *S* parameters for both NUDA designs. To compensate for the condition C_{GS}>C_{DS}, the drain line lengths were larger than the gate line lengths to achieve phase matching between the gate and drain lines. Simulations proved that the optimization of the gate and drain lengths played a crucial role in obtaining high gain and bandwidth. Figure 4 shows the simulated *S* parameters of NUDA with the CS topology. A gain greater than 8dB was obtained over the DC-34 GHz bandwidth range. The Input and Output Return Losses (IORL) were better than -5dB.

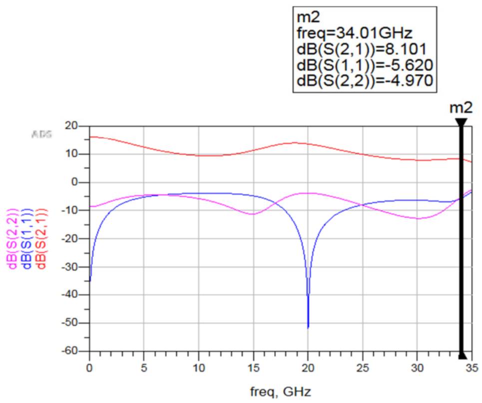

Fig. 4. S parameters of NUDA with CS topology.

The S21 for both 3 and 4 cells was plotted to verify the optimal number of cells, as shown in Figure 5. From the S21 curve, it can be observed that 3 is the optimal number of cells. Figure 6 shows the simulated *S* parameters of NUDA with the Darlington topology. It can be observed that a gain greater than 8dB can be obtained over the DC-38GHz bandwidth. Therefore, bandwidth improved with Darlington topology compared to the CS. The input and output losses were better than -5dB. Figures 7 and 8 show the layouts of NUDA with CS and Darlington topologies, respectively.

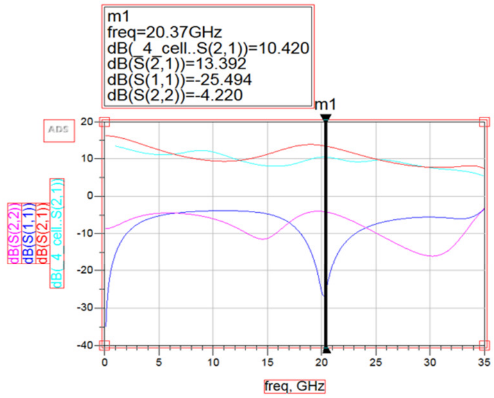

Fig. 5. S21 comparison for 3 and 4 NUDA cells.

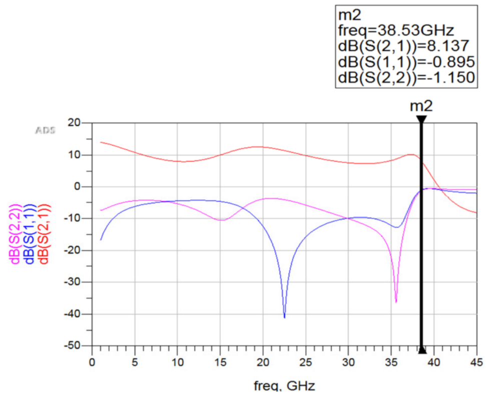

Fig. 6. S parameters of NUDA with Darlington topology.

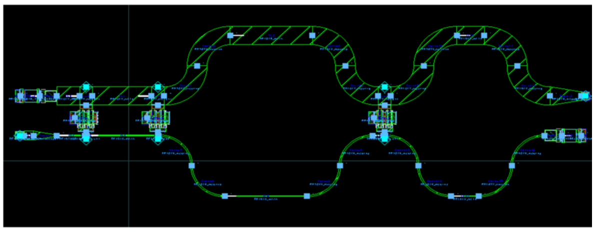

Fig. 7. The layout of NUDA with CS topology.

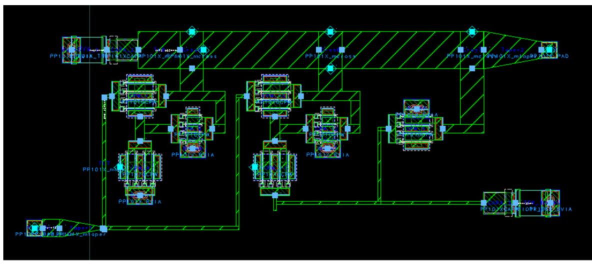

Fig. 8. The layout of NUDA with Darlington topology.

EM simulations were carried out using Keysight's EM solver Momentum Microwave. The EM model was created for the entire design except for the active device. The EM model was imported, and a co-simulation was performed. Table II compares the proposed NUDA with other similar works, where [6-8] used the cascode topology with GaAs HEMT technology.

The proposed design obtained a bandwidth better than [6-7,9]. The DA with the Darlington topology using the CMOS technology [9] obtained a bandwidth of 0.5-23GHz. The proposed design using the GaAs pHEMT technology with the Darlington topology improved the bandwidth to DC-38GHz. Compared to CMOS with Darlington topology [9], the proposed design obtained a wider bandwidth. To the best of our knowledge, this is the first DA of Darlington topology designed with 0.1μm GaAs pHEMT process.

TABLE II. COMPARISON WITH OTHER STUDIES

Ref.	Technology	Topology	Bandwidth (GHz)	Gain (dB)	Power (mw)
2021 [6]	GaAs	cascode	0.01-22	11.5	125.89
2013 [7]	0.5 μm GaAs E/D HEMT	cascode	DC-33	10.6	62
2018 [8]	0.15 μm GaAs pHEMT	cascode	DC-40	13	550
2022 [5]	0.13 μm GaN HEMT	CS	1-42	8	707.94
2012 [9]	0.18 μm CMOS	Darlington	0.5-23	10	150
This work	0.1 μm GaAs pHEMT	CS	DC-34	8-12	319.5
This work	0.1 μm GaAs pHEMT	Darlington	DC-38	8-12	236.5

All the previously mentioned studies used 5 or 6 cells to obtain a bandwidth around 38GHz and a gain around 8dB. The studies with cascoded topologies used extra stability networks at the gate of active devices. However, the proposed designs with proper gate and drain line optimization along with a high transition frequency of 130GHz offered by the WIN pp1010 GaAs HEMT succeeded in obtaining competitive bandwidth and gain with a minimum circuitry, as they used only 3 cells. To the best of our knowledge, no NUDA design of Darlington topology with 0.1μm GaAs HEMT has ever been proposed, and the proposed design in this paper is the first of its kind.

V. CONCLUSIONS

This paper presented two nonuniform distributed amplifier designs using the 0.1 μm GaAs pHEMT process. The CS topology succeeded in obtaining a bandwidth of DC-34GHz with a gain greater than 8dB. The simulation results showed that the Darlington topology achieved a bandwidth of DC-38GHz with a gain greater than 8dB. The obtained input and output return losses were better than -5dB. The power consumption of NUDA with CS topology was 319mW and 236.5mW for the Darlington topology. Both topologies obtained competitive results using the minimum number of three cells of 0.1μm GaAs pHEMT.

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