Efficiency Analysis and Design Considerations of a Hysteretic Current Controlled Parallel Hybrid Envelope Tracking Power Supply

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ABSTRACT

This paper presents the realization of an Envelope Tracking Power Supply (ETPS), for a sinusoidal envelope input signal. A parallel hybrid topology is chosen for the implementation. In this topology, a voltage-controlled Class-AB linear amplifier stage and a current-controlled switching converter stage operate in parallel. A hysteretic current control scheme is employed to control the operation of the switching converter. Block-level implementation of the ETPS is done using Simulink 2017b, continuous mode simulation. Simulations are performed using a sinewave input envelope signal = 1.94+ 1.2 sin(ω·t). The input frequency varied from 1MHz to 60MHz. As the input frequency is increased, the ETPS moves from the linear to the non-linear region of operation. During the transition, the slew rates of the load current and the switching current match at a particular input frequency of 2MHz while the efficiency peaks. The maximum obtained efficiency while tracking the sinewave input signal is 82.3%. The way the efficiency can be optimized by focusing on the matching of the slew rates of load and switching currents is explained. Also, an insight into the study of various circuit parameters and the trade-offs that the designer needs to consider while designing an ETPS, is provided.

Keywords-envelope tracking; RF power amplifiers; supply modulators; ETPS; ETPA; mobile communication; design considerations

I. INTRODUCTION

To cater to the ever-increasing demands of customers, RF power amplifiers in mobile communications need to deal with signals that have a very high Peak to Average Power Ratio (PAPR). Operating such an RF power amplifier with a fixed supply is no longer a viable option, as it reduces the overall efficiency as well as battery lifetime between charges. Envelope tracking is an assuring supply modulation technique [1-4] that helps improving the efficiency of such an RF power amplifier. Envelope Tracking Power Supply (ETPS) is a vital block of an Envelope Tracking Power Amplifier (ETPA), since the overall efficiency of the ETPA [5] depends on the efficiency of the ETPS as given by:

$$\eta_{ETPA} = \eta_{ETPS} * \eta_{RFPA} \quad (1)$$

The primary goal of an ETPS designer is to develop an efficient power supply, operating at higher bandwidths. Various ETPS topologies exist [6-9], aiming to provide high efficiency while maintaining signal fidelity. A hysteretic current controlled parallel hybrid ETPS, as shown in Figure 1, is employed in this paper, as it operates efficiently at high frequencies.

In this topology, a switching converter will track most of the low frequency signals, at high efficiency. The remaining high frequency signals will be tracked by the linear amplifier at a lower efficiency. The linear amplifier stage also needs to compensate for the ripples created by the switching converter, which is controlled by a hysteretic current control mechanism. The hysteretic current control mechanism offers a fast response

since it employs a window comparator and hence is ideal for high bandwidth mobile applications [10-11].

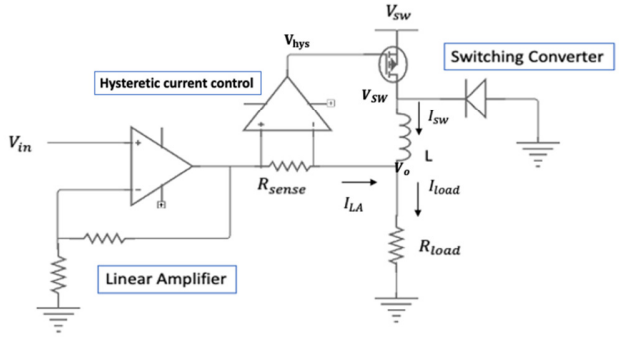

Fig. 1. Hysteretic current controlled ETPS [12].

II. BLOCK LEVEL IMPLEMENTATION OF HYSTERETIC CURRENT CONTROLLED PARALLEL HYBRID ETPS

A block level implementation [13] of hysteretic current controlled parallel hybrid ETPS is depicted in Figure 2. A sinusoidal signal denoted by (2) is provided as the input envelope signal:

$$V_{in}(t) = V_{in\_dc} + V_{in\_ac} \sin(\omega t) \quad (2)$$

where $V_{in}(t)$ is the instantaneous input signal, V_{in_dc} the DC component of the input signal, $V_{in\_ac} \sin(\omega t)$ the AC component of the input signal, and $\omega = 2\pi . f_{i/p}$, where $f_{i/p}$ is the input signal frequency.

A Class AB amplifier with an operational trans conductance amplifier input stage is used as the linear stage, as shown in Figure 3. A single stage buck converter is used as the switching stage, as shown in Figure 4.

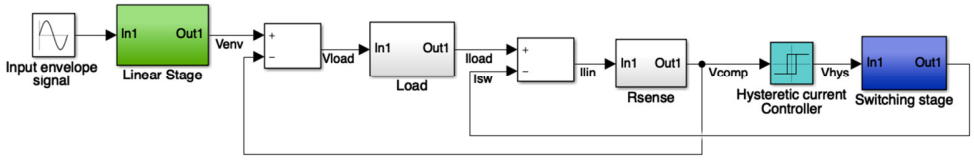

Fig. 2. Block level implementation.

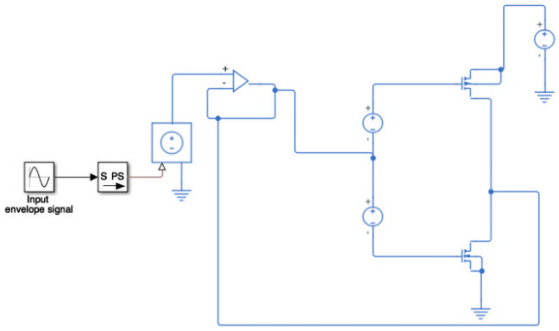

Fig. 3. Linear stage.

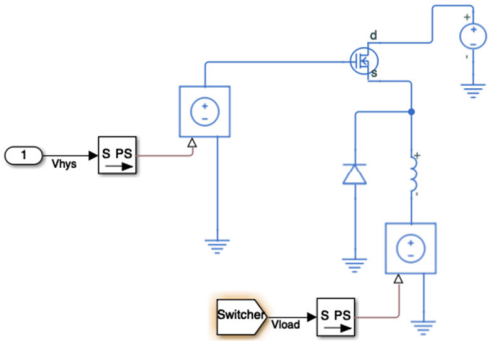

Fig. 4. Switching stage.

Linear stage current, I_{LA} is sensed by the resistor R_{sense} and the direction of this current controls the operation of the Hysteretic Controller. The value of R_{sense} is kept very small in order to sense the current accurately. A relay block in Simulink is used to function as a hysteretic controller. Hysteresis h is chosen to be equal to ±7mV. Initially, the linear stage starts [14-18], providing current and when the voltage drop across the R_{sense} exceeds +7mV, the hysteretic controller will turn ON the switching converter. The switching stage starts providing the majority of the load current, as given by (3). The linear stage needs to source only the difference current during this time.

$$I_{load} = I_{SW} + I_{LA} \quad (3)$$

As the current provided by the switching stage increases and when the I_{SW} exceeds the I_{load}, the current through R_{sense} starts flowing in the opposite direction. When the voltage drop across R_{sense} falls below -7mV the hysteretic controller turns the switching converter OFF. The linear stage now needs to sink current.

III. REGIONS OF OPERATION OF HYSTERETIC CURRENT CONTROLLED PARALLEL HYBRID ETPS

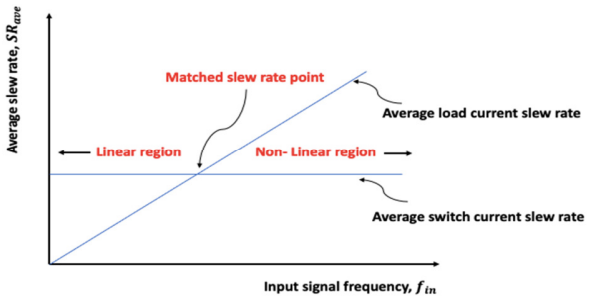

Fig. 5. Regions of operation.

The working of the hysteretic current controlled [19-24] Parallel Hybrid ETPS can be explained in 3 regions, as shown

in Figure 5. The circuit parameters considered for performing simulations in the 3 operating regions are mentioned in Table I.

TABLE I. PARAMETERS CONSIDERED FOR SIMULATION

Parameter	Value
Input envelope signal	V_s=1.94+1.2 sin(2. π.$f_{i/p}$.t)
R_{sense}	1Ω
R_{load}	47Ω
L	11µH
h	± 7mV
V_{dd}	5.5V

A. Linear Region of Operation

In this region of operation, the slew rate of switching current is greater than the slew rate of load current as represented by (4).

$$\text{SR } i_{sw} > \text{SR } i_{load} \quad (4)$$

Simulations were conducted at 1MHz input frequency and the obtained results are shown in Figure 6. It can be observed that the slew rate of the switching current is greater than that of the load current. As a result, the switching frequency f_s of the switching stage increases and the calculated average switching frequency of the buck converter is 6.6MHz. The linear stage current is within the hysteresis values of ±7mA.

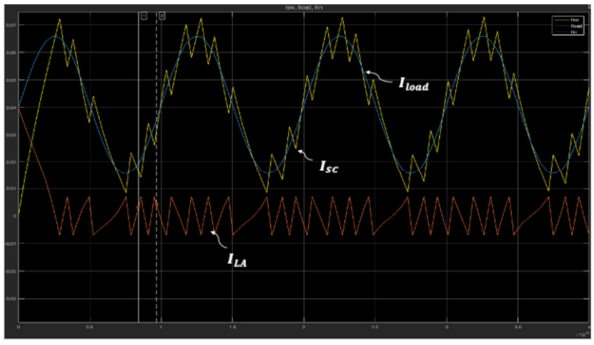

Fig. 6. I_{LA}, I_{SW}, I_{load} at 1MHz f_{in}.

The load current is the sum of linear stage current and the switching stage current, as is clearly visible from Figure 6. When the inductor current I_{sw} is rising, the current provided by the linear amplifier decreases and vice-versa. Hence, the three currents obey (5):

$$I_{SW}(t) + I_{LA}(t) = I_{load}(t) \quad (5)$$

$$I_{SW}(t) + \frac{V_{in}(t) - V_o(t)}{R_{sense}} = \frac{V_o(t)}{R_{load}} \quad (6)$$

Now, the switching current is:

$$I_{SW}(t) = I_{SW\_noise}(t) + I_{SW_{input\ signal}}(t)$$

$$= I_{SW\_noise}(t) + \frac{V_{in}(t)}{R_{load}} \quad (7)$$

Substituting the (7) in (6), we get:

$$V_o(t) - V_{in}(t) = R_{sense} \cdot I_{SW\_noise}(t)$$

$$I_{SW\_noise}(t) = \frac{V_o(t) - V_{in}(t)}{R_{sense}} \quad (8)$$

This ripple current needs to be absorbed by the linear stage and, hence, the ripple voltage due to the switching current is given by:

$$I_{SW\_noise}(t) \cdot R_{sense} = V_o(t) - V_{in}(t) \quad (9)$$

The corresponding ripple voltage, $V_o(t) - V_{in}(t)$ obtained during the simulation is given in Figure 7. It can be observed that the ripple voltage falls within the hysteresis value of ±7mV.

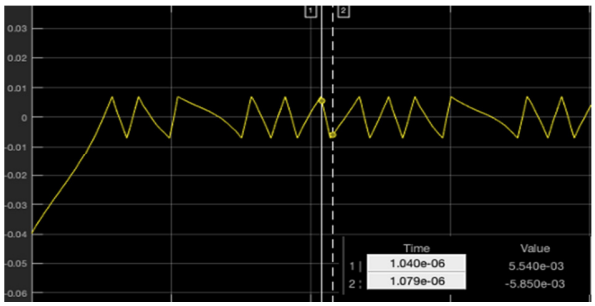

Fig. 7. Ripple voltage at 1MHz f_{in}.

B. Matching Slew Rate Point

The slew rate of the switching current is equal to the slew rate of the load current in this operating region, as given by (10):

$$\text{SR } i_{sw} = \text{SR } i_{load} \quad (10)$$

The simulation results at 2MHz input frequency are given in Figure 8.

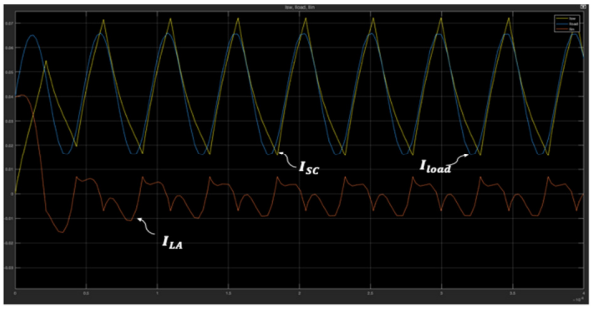

Fig. 8. I_{LA}, I_{SW}, I_{load} at 2MHz f_{in}.

The average switching frequency of the converter is calculated to be 2MHz, which is equal to the input frequency. The linear stage current is slightly higher than the hysteresis values. The switching frequency is observed to be minimum at this point. The obtained corresponding ripple voltage is given in Figure 9. It can be observed that error is slightly greater than the hysteresis value of ±7mV.

C. Non-Linear Region of Operation

In this operating region, the slew rate of the switching current is lower than the slew rate of the load current as represented by (11):

$$SR\ i_{sw} < SR\ i_{load} \quad (11)$$

Simulations were conducted at 20MHz input frequency and the resulting current waveforms are given in Figure 10. As can be observed, the switching stage is able to provide only the DC components of the load current. The linear stage needs to provide the AC components of the load current. The average switching frequency of the converter is calculated to be 20MHz.

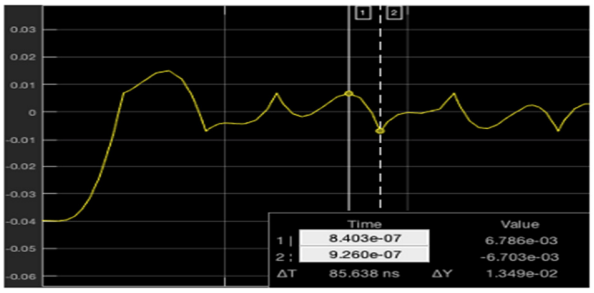

Fig. 9. Ripple voltage at 2MHz f_{in}.

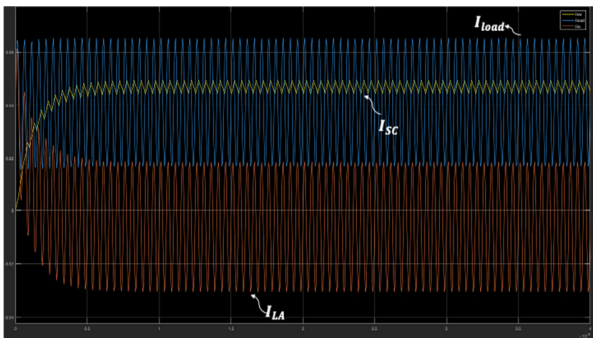

Fig. 10. I_{LA}, I_{SW}, I_{load} at 20MHz f_{in}.

The error ripple voltage obtained during the simulation is given in Figure 11. It can be observed that the error has significantly increased.

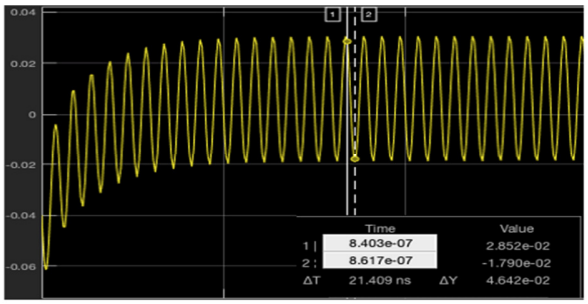

Fig. 11. Ripple voltage at 20MHz f_{in}.

IV. EFFICIENCY AND LOSS ANALYSIS OF ETPS

The efficiency of an ETPS is given by (12):

$$\eta_{ETPS} = \frac{P_{out(av)}}{P_{out(av)} + LA_{losses} + SC_{losses}} \quad (12)$$

where $P_{out(av)}$ is the average output power of the ETPS, LA_{losses} represents the losses occurring in the linear amplifier stage, and SC_{losses} the losses occuring in the switching converter stage.

A. Linear Stage Losses

Class AB linear stage comprises of NMOS and PMOS devices, referring to Figure 3 and the occurring total losses are the sum of the losses in NMOS and PMOS devices, as stated in (13):

$$LA_{losses} = NMOS_{losses} + PMOS_{losses} \quad (13)$$

where:

$$NMOS_{losses} = (I_{SW} - I_{load})\ V_{out}$$

$$PMOS_{losses} = (I_{load} - I_{SW})\ (V_{dd} - V_{out})$$

B. Switching Stage Losses

Switching stage losses comprise of conduction losses in the diode and MOSFET, switching losses in the MOSFET, and driver losses:

$$SA_{losses} = Conduction_{losses} + Switching_{losses} + Driver_{losses} \quad (14)$$

where:

$$Conduction_{losses} = ON\_diode_{losses} + ON\_MOS_{losses} \quad (15)$$

$$ON\_diode_{losses} = (1 - D).\ I_{SW\_dc}.\ V_{on\_diode}$$

where $D = V_{out\_dc} / V_{dd}$.

$$ON\_MOS_{losses} = D.\ I_{SW\_dc}{}^2.\ R_{on} \quad (16)$$

where R_{on} is the ON resistance of the MOSFET.

$$Switching_{losses} = I_{SW}\ .\ V_{off}\ .(t_{on} + t_{off})\ f_{sw\_ave}\ /2$$

where $t_{on} = \frac{C_G V_G}{I_{driver(L \rightarrow H)}}$ and $t_{off} = \frac{C_G V_G}{I_{driver(H \rightarrow L)}}$.

$$Driver_{losses} = Q_g\ V_{gs}\ f_{sw\_ave} \quad (17)$$

Linear region of operation:

$$f_{sw\_ave} = \frac{R_{sense}}{L} \frac{V_{dd}}{2.h} D\ (1\text{-}D.\ \frac{V_{s\_rms}{}^2}{V_{s\_dc}{}^2})$$

Non-linear region of operation:

$$f_{sw\_ave} = f_{i/p}.$$

V. ETPS SIMULATION MEASUREMENTS FOR VARYING INPUT FREQUENCY

V_{in}= 1.94+ 1.2 sin(2. π.$f_{i/p}$ t) is the input signal considered for simulation. The input frequency $f_{i/p}$ is varied over a wide range from 1MHz to 60MHZ. Correspondingly, the average switching frequency of the switching converter, f_{sw} is noted down. Linear amplifier and switching converter losses are also obtained (Table II). The efficiency is calculated by (12).

It can be observed that the efficiency peaks at an input frequency of 2MHz. At this frequency, $SR\ i_{sw} = SR\ i_{load}$ and f_{sw} is minimum. As a result, switching losses are minimum, as highlighted in Table II and the efficiency peaks, as shown in

Figure 12. For $f_{i/p}$ lower than 2MHz, $SR\ i_{sw} > SR\ i_{load}$ and hence the increased switching losses result in lowering the efficiency. For $f_{i/p}$ higher than 2MHz, $SR\ i_{sw} < SR\ i_{load}$. In this condition, the switching converter will be able to provide only the DC components of the load current. As a result, the linear amplifier needs to provide the AC components, which results in increased linear stage losses and consequently, a drop in efficiency. Hence, the efficiency of a hysteretic current controlled parallel hybrid ETPS drops as the input signal frequency increases.

TABLE II. EFFICIENCY ANALYSIS FOR VARYING INPUT FREQUENCY

f_{in} (MHz)	f_{sw} (MHz)	P_{out} (W)	LA_{losses} (W)	SC_{losses} (W)	η
1	6.6	0.094	0.00077	0.02151	80.8%
2	2	0.093	0.00217	0.0179	82.3%
5	5	0.094	0.03706	0.02333	60.9%
10	10	0.093	0.03915	0.02825	58.2%
20	20	0.093	0.03920	0.03821	54.6%
40	40	0.092	0.03906	0.05799	48.8%
60	60	0.093	0.03981	0.07759	44.2%

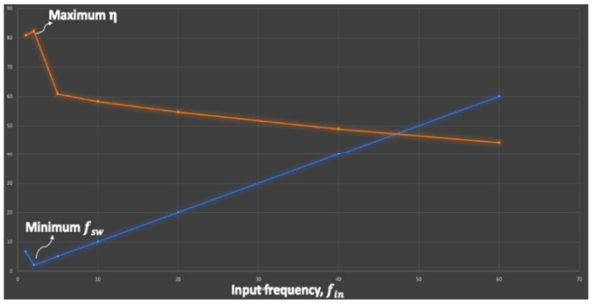

Fig. 12. Input frequency versus switching frequency and efficiency.

VI. DESIGN CONSIDERATIONS

Various parameters like R_{sense}, R_{load}, L, h, V_{dd} need to be analyzed and considered while designing an ETPS. The main goal of an ETPS designer is to accurately reproduce the input envelope signal at maximum circuit efficiency. R_{sense} is chosen to be very much smaller then R_{load} to reduce the losses occurring in the current sense resistor. Inductor L, hysteresis h, and supply voltage V_{dd}' are parameters determined by the designer. The simulations conducted in Section V are taken as the base to study the variations in efficiency with respect to parameter variations. The Input signal considered is:

$$V_{in}= 1.94+ 1.2 \sin(2.\pi.f_{i/p}\ t)$$

A. Inductor, L Variations

The inductor value selected for simulation in Section V was 11µH. The average slew rate of the switching current is given by (18):

$$SR_{isw\_ave}=\frac{2}{L}\left(1-\frac{V_{in\_dc}}{V_{dd}}\right)V_{in\_dc} \quad (18)$$

Reducing the inductor value to 5µH increases the slew rate of the switching current. $SR\ i_{SW}$ exceeds $SR\ i_{load}$ and hence SA_{losses} increases as shown in Table III. This brings down the efficiency. Increasing the inductor value to 30µH reduces the slew rate of the switching current. $SR\ i_{SW}$ goes below $SR\ i_{load}$ as shown in Figure 13. As a result, the switching stage will be able to provide only the DC components of the load current and the linear stage will be forced to provide the AC components. This increases the losses occurring in the linear stage and consequently lowers the efficiency.

TABLE III. EFFICIENCY ANALYSIS FOR VARYING INDUCTOR VALUES

f_{in} = 2 MHz				
L (µH)	f_{sw} (MHz)	LA_{losses} (W)	SC_{losses} (W)	η
5	6.69	0.0007802	0.02147	80.1%
12	2	0.002172	0.01798296	82.3%
30	6.7	0.03757	0.02386	60.05%

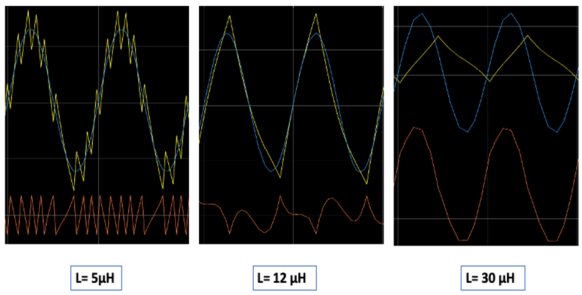

Fig. 13. Changes in slew rate as L changes.

B. Hysteresis Variations

The hysteresis value selected for the simulation was ±7mV. When it reduces to ±2mV, the switching frequency increases tremendously and hence the switching losses increase as shown in Table IV. As a result, the efficiency drops. When the hysteresis value increases to ±20mV, the switching frequency of the converter reduces drastically and the switching converter now fails to provide the entire load current. As mentioned above, this results in increased losses occurring in linear stage. Efficiency again drops.

TABLE IV. EFFICIENCY ANALYSIS FOR VARYING HYSTERESIS VALUES

h (mV)	LA_{losses} (W)	SC_{losses} (W)	η
2	0.006895	0.02237	76.3%
7	0.002207	0.01798	82.3%
20	0.03045	0.02001	65.1%

C. V_{dd} Variations

The selected V_{dd} for simulations in Section V is 5.5V. The average slew rate of the switching current is given by (16). Simulations are performed at 1MHz input frequency and the corresponding slew rates can be observed in Figure 14. The corresponding average switching frequency obtained from simulations is 8MHz. As the V_{dd} drops to 4.5V, the SR_{isw_ave} drops as shown in Figure 15. The corresponding average switching frequency obtained from simulations is reduced to 6MHz.

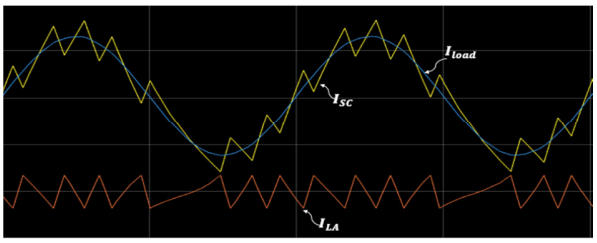

Fig. 14. SR_{isw} and SR_{iload} at V_{dd} =5.5V.

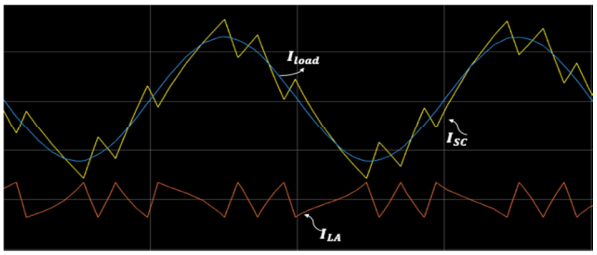

Fig. 15. SR_{isw} and SR_{iload} at V_{dd} =4.5V.

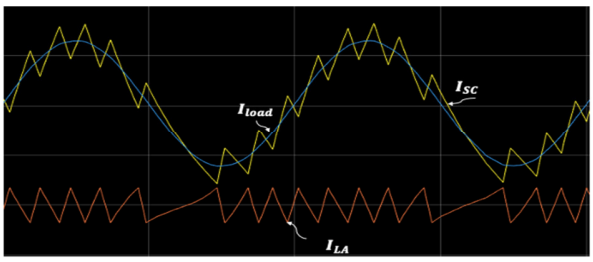

Fig. 16. SR_{isw} and SR_{iload} at V_{dd} =6.5V.

As the V_{dd} increases to 6.5V, the SR_{isw_ave} increases as shown in Figure 16. The obtained corresponding average switching frequency has increased to 9MHz. Hence, by varying the supply voltage V_{dd} of the switching converter, the slew rates of the switching current can be varied to match with the slew rates of the load current and thereby to obtain maximum efficiency.

VII. CONCLUSION

The current paper presents a novel idea to the hysteretic current controlled parallel hybrid ETPS designers, that they should focus on matching the slew rates of switching and load currents for all frequencies of operation, in order to obtain maximum efficiency at all operating frequencies. In this paper, the hysteretic current controlled parallel hybrid ETPS is implemented in Simulink and simulations were performed using a sinusoidal envelope input signal. Efficiency analysis is performed by varying the input frequency from 1MHz to 60MHz. It was observed that the efficiency peaks for an input frequency of 2MHz, when the slew rates of the load current and the switching current matches. Ripple voltage was found to be increasing from 5.5mV to 28mV as the region of operation moved from linear to non-linear. Various circuit parameters that the designer needs to consider while designing an ETPS and its trade-offs are also discussed in length. The simulated ETPS could work for a peak efficiency of 82.3% for a switching frequency of 2MHz, while tracking the sinusoidal envelope input signal at 2MHz input frequency. One major advantage of the current work is that it is using a single level switching converter whereas most of the existing works are using multi-level switching converters, which increases complexity.

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