Implementation of a High Power Quality BLDC Motor Drive Using Bridgeless DC to DC Converter with Fuzzy Logic Controller

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Abstract-Electric motor drives based on electronic power converters having good power quality parameters are getting huge acceptance. Conventional Diode Bridge Rectifier (DBR) and DC to DC converter-based methods have become obsolete, as they provide low power quality indices which hamper the supply by introducing current harmonics and conduction losses. Although there are many developments in motors and control strategies, the risk and complexity of such drives become bottlenecks in implementation. This study implemented a drive scheme with a brushless DC Motor. The new improved bridgeless topology was modified with an advanced fuzzy logic controller to further improve its power quality and performance. Due to low power, a high-speed application of Brush Less (BLDC) motor was selected for the drive scheme. This combination could achieve almost Unity Power Factor (UPF) and significantly improve control compared to conventional topologies. A circuit-wise analysis was conducted to design the converter's components. The modifications were elaborated through mathematical expressions, and the parameters of power quality were analyzed and validated.

Keywords-Brush-Less Direct Current Motor (BLDC); Diode Bridge Rectifier (DBR); High-Frequency Transformer (HFT); Total Harmonic Distortion (THD); Discontinuous Inductor Current Mode (DICM); Bridgeless Dual Cuk (BDC); Fuzzy Logic Controller (FLC); Unity Power Factor (UPF)

I. INTRODUCTION

The need for quality AC supplies and their efficiency is becoming a primary concern in modern power electronics [1], especially in the development of various DC-DC and AC-DC converters. This paper discusses DC-DC converters, as they are more flexible and versatile in terms of power quality and efficiency. Improved power quality is mandatory for electrical equipment nowadays by the international Power Quality (PQ) standard IEC 61000-3-2. This standard also stipulates high power factor and low Total Harmonic Distortion (THD) of the AC main current for Class-A applications (<600W, <16A) [2]. Due to their advantages of high efficiency, high flux density per unit volume, low maintenance requirement, low EMI problems, high ruggedness, and a wide range of speed control, Brush-Less DC (BLDC) motors are recommended for many low- and medium-power drive applications [3]. BLDC motors are used in numerous areas such as household applications [4], transportation (hybrid vehicles) [5], aerospace [6], heating, etc.

This study implemented and evaluated a variety of power electronic circuits to drive a BLDC motor. An AC Supply is essential for domestic loads. Conventionally, a Diode Bridge Rectifier (DBR), followed by a filter capacitor is used for the generation of a DC supply. Today, many applications continue to use them due to their simplicity of construction and cost-effective production. The high value of the filter capacitor draws a high non-sinusoidal current from the supply. In addition, DBRs with their inherent flaw of high conduction losses reduce the efficiency of converter circuits, and increased harmonic levels cause a rise in the THD levels between 45-65% [7]. Many Power Factor Correction (PFC) converters have been developed to reduce the THD levels to permissible limits and improve the power factor of the supply, and most of them serve their purpose on their performance levels. Therefore, more reliable drive control is performed through the control of the DC link voltage by controlling the switches on the PFC converter side [8]. To implement such a control, the converter has to be chosen from an array of DC-DC converters divided into isolated or nonisolated and bridged or bridgeless topologies [9, 10]. Moreover, it has to be decided in which mode the converter should operate to achieve Unity Power Factor (UPF).

This study selected a Cuk converter, after examining various topologies with different types of loads and applications of PFC converters, intending to improve the power quality of AC to DC conversion. This study also presents the bridgeless topology with a proposed modification. Additionally, a fuzzy logic-based advanced linguistic controller was implemented for the bridgeless topology to further enhance the performance of the converter and improve power quality at the main supply. The simulated results along with their mathematical validation, were used to analyze the improvements. Performance analysis and input power quality

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of the operation of the converter were used to conduct the harmonic analysis of the topology. As there are many speed control drive schemes for various applications, this study allowed the operation of a motor drive with quick response and very low speed variations from the reference value. Moreover, the incorporation of FLC into a bridgeless configuration further improved performance and power quality.

II. CONFIGURATION

For speed control, the selection of the front-end converter and its operation configuration are equally important to achieve a high power factor at the supply mains. The Cuk converter was selected due to its many advantages [12]. There are multiple approaches for the conversion of AC input to variable DC for the drive scheme. A DBR followed by a high DC link capacitor was used, which due to its high losses was replaced by "DBR-Power Factor Correction (PFC)" converter configuration. In such circuits, the speed control of the drive can be achieved in several ways. One way is to control the switching of the 6 individual switches of the motor-end Voltage Source Inverter (VSI). Due to the increased number of control switches and the high frequency of motor operation, it is not preferred due to high switching losses [8]. Another solution could be a PFC converter to control the DC link voltage. The PFC converter can be controlled by 2 methods: a voltage follower or a current multiplier method [13]. These methods depend on which mode the PFC converters operate. This study discussed the 2 modes of operation and attempted to compare their results with the bridgeless topology. PID controllers were used for the three types of converters, using a linearized modeling technique to standardize the results.

In the voltage follower approach [13], the converter operates in DCM and is further divided into DICM and DVCM where the respective inductor currents or capacitive voltages become discontinuous during a switching period of the converter switch [13]. The advantage of this mode is that it requires only one sensor for control. The need for 2 voltage sensors and 1 current sensor makes this multiplier method more complex [13]. In this configuration, the converter operates in CCM and ensures more robust control [14]. The configuration consists of a DBR followed by a power factor correction Cuk converter designed to operate in CCM operation. The DC output of the converter is fed to the input side of the voltage source inverter that controls the speed of the BLDC motor. Even though both configurations have their advantages, the main drawback of lack of isolation between the high- and low-frequency switching parts hampers the smooth operation by introducing harmonics in the circuit. This reduces the converter's efficiency and the purported operation in power factor correction.

The proposed configuration, shown in Figure 1, resolves this inherent problem by providing high-frequency isolation [9]. This is done by providing 2 High-Frequency Transformers (HFT) in the respective positive and negative side converters of the modified Cuk converter topology. The modification of the proposed converter eliminates the need for a DBR and avoids any conduction losses. The converter operates in DICM, where the current through the output side inductor becomes discontinuous over a switching period. Three converters were constructed and analyzed in Matlab 2018 and their performance was compared during changes in speed conditions.

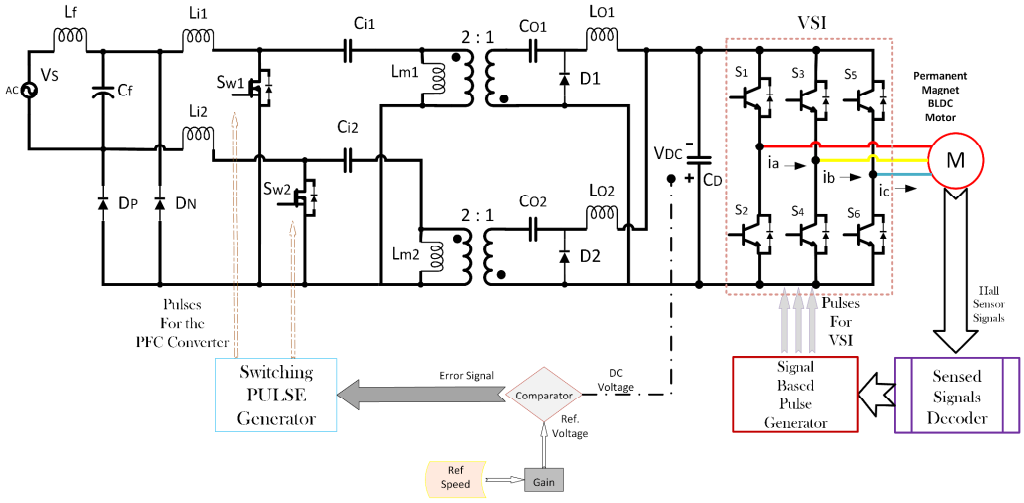

Fig. 1. Proposed isolated coupled Cuk converter-fed BLDC motor drive

III. OPERATION OF THE CONFIGURATION

The input side DBR was eliminated in the proposed converter-fed BLDC motor drive. This was achieved by incorporating another Cuk converter in parallel with the existing one so that one works in the positive half-cycle and the other in the negative half-cycle of the supply, by implementing a zero-crossing detector on the input side. Another major advantage of this method was that the AC input and the output side BLDC motor drive were completely isolated with the help of an HFT. Hence, the speed control of the drive was hassle-free and the amount of noise present in the control signals could also be reduced. The converter was designed in such a way that the current through the output inductors *Lo1* and *Lo2* becomes discontinuous over a switching period in either half cycle of the input supply, as shown in Figure 2. Therefore, the converter operated in Discontinuous Inductor Current Mode

(DICM) [15]. Even though there are many categories of discontinuous conduction modes, such as DICM on input, DICM on output, and DCVM [16], applying DICM on the output side inductor was simpler and lowered harmonics. Several advantages can be gained by operating the rectifier in DICM, such as a natural near-unity power factor and at zero current the power switches are turned ON and the output diodes are turned OFF.

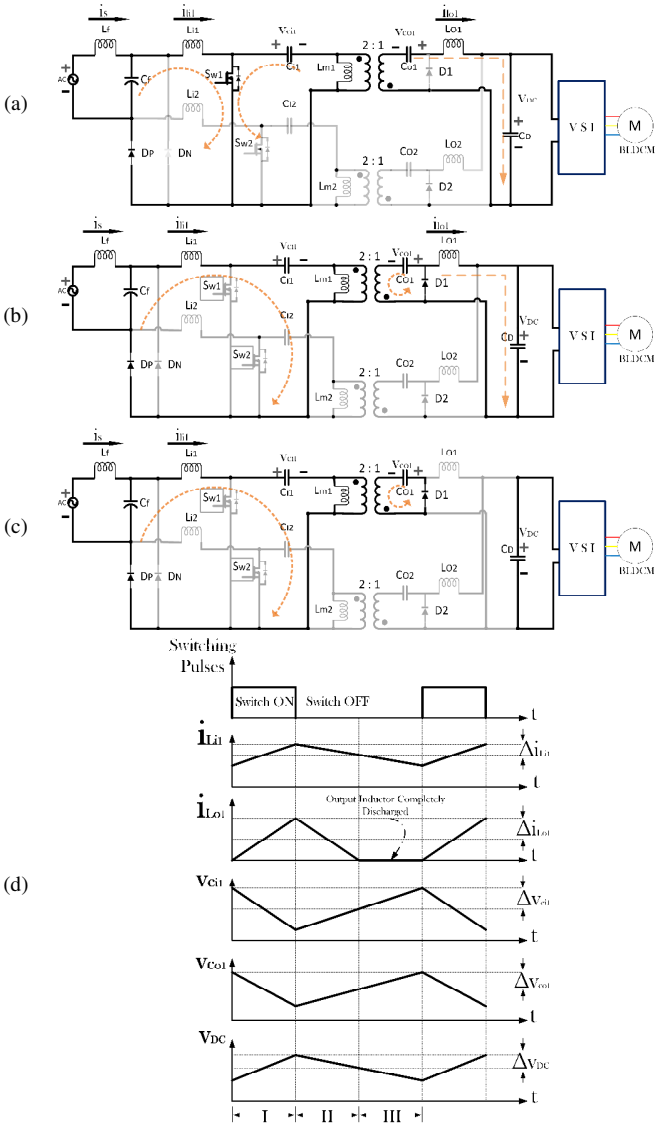

Fig. 2. Operating modes of the proposed converter at different intervals of the switching period during the positive half cycle: (a) switch closed, (b) switch open – inductor discharging, (c) switch closed – inductor fully discharged, and (d) associated waveforms.

In the first mode, switch *Sw1* is turned ON and the inductors *Li1*, *Lo1*, and magnetizing inductance *Lm1* start charging. The capacitor *Ci1* charges *Lm1*, and *Co1* delivers DC link voltage. In the second mode, the switch is being turned OFF, inductors *Li1* and *Lo1* discharge thereby charging *Ci1* and *Co1,* and the magnetizing inductance *Lm1* discharges through *Cd*. In the third mode, the output side inductor *Lo1* is completely discharged and the input inductor *Li1* and the magnetizing inductance of HFT *Lm1* continue to discharge. Figure 3 shows the negative half operation of the converter. The converter operates in such a way that the input side energy storage components remain in non-conducting mode and the output side components remain non-discharged. The converter is designed so that the positive sinusoidal input from the AC supply at the fundamental frequency of 50Hz is split into a large number of cycles of operation of the upper Cuk converter switch.

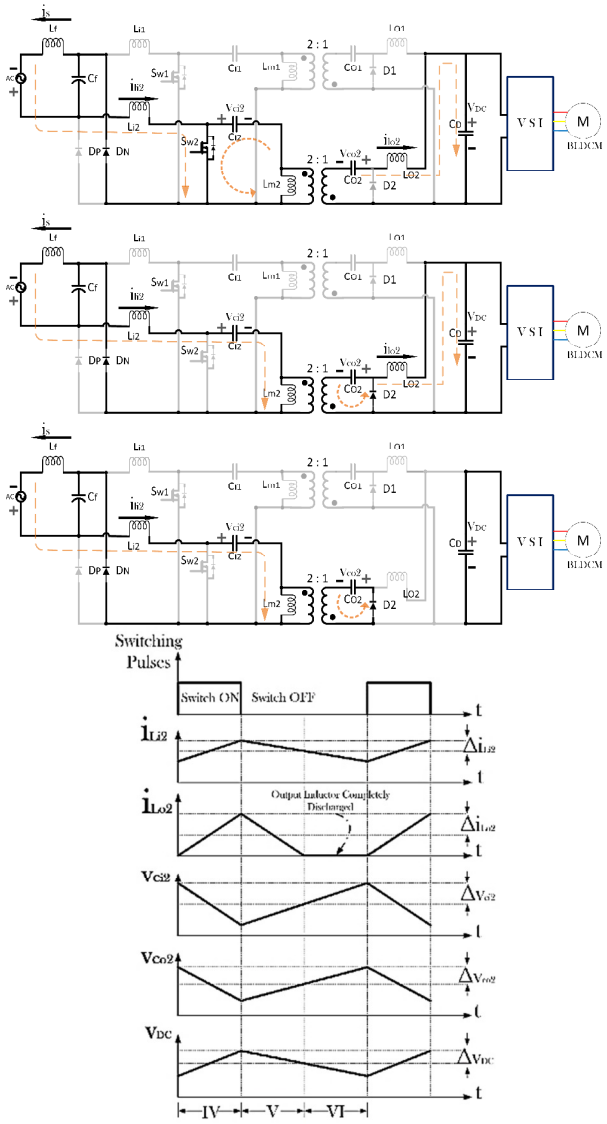

Fig. 3. Operating modes of the proposed converter at different intervals of switching period during the negative half cycle: (a) switch closed, (b) switch open – inductor discharging, (c) switch closed – inductor fully discharged, and (d) associated waveforms.

A. Motor Speed Control

An electronic commutation of the BLDC motor includes the proper switching of the Voltage Source Inverter (VSI) to

draw a symmetrical DC from the DC link capacitor for 120° [17] and placed symmetrically at the center of the back Electro-Motive Force (EMF) of each phase. A Hall-effect position sensor was used to sense the rotor position on a span of 60°; which is required for the electronic commutation of the BLDC motor [18]. The front-end converter was controlled by feeding back the DC voltage. The control scheme was comprised of feedback DC voltage, reference voltage generator, and PWM generator. The reference voltage was obtained by multiplying the reference speed by the motor speed constant K_v:

$$V_{DC}{}^{*} = K_v \,.\, \omega$$

This reference voltage was compared with the actual DC link value of the converter and the error was used for PWM generation in 3 different ways for the front-end converter switches to obtain speed control [19]. Table I illustrates the switching signals to be sent to the phase 3 VSI. The controller logic was designed to send the ON pulses to the respective switches following the rotor position in a single direction.

TABLE I. SWITCHING STATES FOR THE VSI

Angular Placement	State of Switches					
	T1	T2	T3	T4	T5	T6
NA	0	0	0	0	0	0
0-60	0	0	0	1	1	0
60–120	0	1	1	0	0	0
120–180	0	1	0	0	1	0
180–240	1	0	0	0	0	1
240–300	1	0	0	1	0	0
300–360	0	0	1	0	0	1
NA	0	0	0	0	0	0

IV. DESIGN

The basic CUK converter is shown in Figure 4.

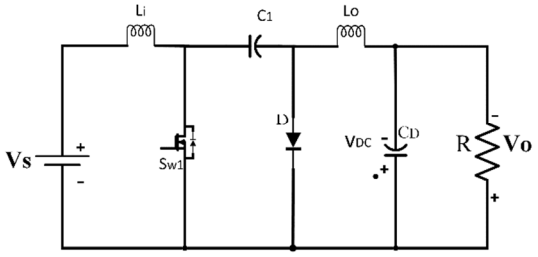

Fig. 4. CUK converter circuit.

For this Cuk converter, the output equation is given as [21]:

$$V_{DC} = - \frac{D}{1-D} V_{in}$$

In the case of the shown converter topology, the negative output at the output changes to a positive value by interchanging the terminals. In this type of arrangement, the average AC voltage applied across the input side can be obtained as:

$$V_{in}(t) = |V_m \sin(\omega t)| = \left|230\sqrt{2}\sin(340t)\right| \quad (1)$$

using the following parameter values: V_{min}=100V, V_{max}=200V, Vs_{min}=170V, Vs_{max}=270V, P_{max}=250W, and P_{min}=125W. The selected switching frequency *fs* was 20kHz for the operation of all 3 converters.

A. Design of the BDC Converter

The output voltage is obtained as [21]:

$$V_{DC} = \left[\frac{N_2}{N_1}\right] \frac{D}{(1-D)} V_{in} \quad (2)$$

Transformer ratio, $\left[\frac{N_2}{N_1}\right]$ was taken as 0.5. Let $D(t)$ be the instantaneous value of the duty ratio, then we have [16]:

$$D(t) = \frac{V_{DC}}{\left(N_2/N_1\right)V_{in}(t)+V_{DC}} = \frac{V_{DC}}{\left(N_2/N_1\right)*|V_{in}\sin(\omega t)|+V_{DC}} \quad (3)$$

Instantaneous power is given by:

$$P_i = \left(\frac{P_{max}}{V_{DC\_max}} V_{DC}\right) \quad (4)$$

1) Inductor Design [20]:

$$L_{i1} = L_{i2} = \frac{V_{in}(t).D(t)}{\eta I_{in}(t) f_s} = \frac{1}{\eta.f_s}\left(\frac{V_s{}^2}{P_i}\right)\left(\frac{V_{DC}}{nV_{in}(t)+V_{DC}}\right) \quad (5)$$

where η is the input current ripple, which was taken as 50%, and *n* is the turns ratio of the HFT, taken as 1:2.

$$L_{o1} = L_{o2} = \left(\frac{V_s{}^2}{P_i}\right)\frac{V_{DC}}{2V_{in}(t)f_s}\left(\frac{V_{DC}}{nV_{in}(t)+V_{DC}}\right) \quad (6)$$

Both equations are used under the assumption that P_i=$P_{i\text{-}max}$ and V_{in}=$\sqrt{2}\,V_{s\_min}$.The value of the input side inductor was 7mH. The value of the output side inductor was obtained as 1.502mH for *VDC*=200V, and 0.546mH for *VDC*=100V, so a value lower than 0.546mH should be chosen. The selected value selected was 0.1mH. The magnetizing inductances are [16]:

$$L_{m1} = L_{m2} = \left(\frac{V_s{}^2}{P_i}\right)\frac{1}{\varsigma.f_s}\left(\frac{V_{DC}}{nV_{in}(t)+V_{DC}}\right) \quad (7)$$

where ς is the permitted ripple current on the output side, taken as 50%, were obtained as 7mH.

2) Capacitor Design

$$C_{i1} = C_{i2} = \frac{n.P_i}{k.\sqrt{2}V_s.f_s.(n\sqrt{2}V_s+V_{DC})} \quad (8)$$

where *Ci1*=*Ci2*=220nF.

$$C_{o1} = C_{o2} = \frac{P_i}{x.V_{DC}.f_s(n\sqrt{2}V_s+V_{DC})} \quad (9)$$

where *Co1*=*Co2*=2.2μF. The output side DC link capacitor was given as:

$$C_D = \frac{I_{DC}}{2\omega\Delta V_{DC}} = \left(\frac{P_i}{V_{DC}}\right)\frac{1}{(2\omega.\rho.V_{DC})} \quad (10)$$

where *k* is the input side ripple voltage (25%), *x* is the ripple voltage at the converter side (10%), and ρ=ΔV_{DC} is the permitted output ripple (5%). The obtained value of *CD* was 1000μF.

3) Filter Design

A low pass LC filter was used to avoid higher order harmonics in the supply system. The maximum value of the filter's capacitance was given by [13]:

$$C_{max} = \frac{I_m}{\omega_L V_m} \tan\theta = \frac{\sqrt{2}\, P_{max} / V_s}{\omega_L \sqrt{2}\, V_s} \tan\theta \quad (11)$$

where θ is the displacement angle between the fundamental value of supply voltage and supply current, taken as 2°. The maximum value of the filter capacitor was calculated using (11) at 574.4nF and was selected as 330nF. This value was selected for all 3 configurations as there is no variation in input voltage, and the capacitor always acts across one-half of the input supply at any given time. The value of the filter inductor was designed by considering the source impedance *Ls* as 4-5% of the base impedance. Hence, the additional value of required inductance was given as:

$$L_f = L_{req} + L_s \Rightarrow L_{req} = L_f - L_s$$

$$L_{req} = \frac{1}{4\pi^2 f_c^2 C_f} - 0.025\left(\frac{1}{\omega_L}\right)\left(\frac{V_s^2}{P_o}\right) \quad (12)$$

where f_c is the cut-off frequency, selected such that $f_L < f_c < f_s$. Therefore, f_c was taken as $f_s/10$. Hence, the value of filter inductance was calculated using (20) as 3.77mH. Table II shows the motor operation details of the proposed topology.

TABLE II. MOTOR SPECIFICATIONS

Number of Poles	4
Rated Power	251.32 W
DC Rated Voltage	200V
Rated Torque	1.2Nm
Rated Speed	2000rpm
Back emf Constant, *Kb*	78V/Krpm
Torque Constant, *Kt*	0.74Nm/A
Per Phase Resistance	14.56Ω
Per Phase Inductance	25.71mH
Moment of Inertia, *J*	1.3×10^{-4}Kgm^2

V. FUZZY LOGIC CONTROLLER

The conventional PID controller has the inherent flaw of the limitation of operation range as it can only be tuned for a particular range or input-output combinations. The FLC [22], which uses linguistic variables to specify the wide range of inputs as its Membership Functions (MFs) can solve this problem of the PID controller and can operate effectively under the complete specified range of the DC voltage of the converter. The voltage range is split into segments and each segment is provided as a MF for the reference voltage and the actual output variables. These variables are considered the input variables of the FLC. Table III and Figures 5 and 6 illustrate the association of MFs to the two inputs to the FLC. From the inputs, FLC calculates the error and, based on the rule base shown in Table IV, it provides the apt duty ratio of the switching pulse, which is to be given to the converter switches. Duty ratios, ranging from 0 to 0.5, are divided into FLC MFs for the defuzzified output variable, as shown in Figure 7. Table V shows the fuzzy rule base defined for the FLC [23]. The selection of an appropriate output for the converter pulse duty ratio is decided on the error between the reference and the actual DC output voltage of the converter. The weightage and the point of selection of the exact value are decided based on the centroid method of FLC.

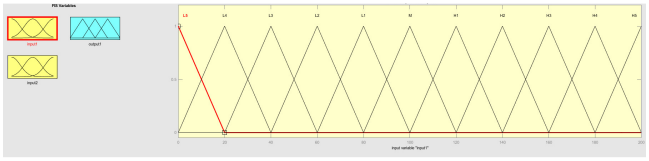

Fig. 5. Input 1 (ref. voltage) membership functions.

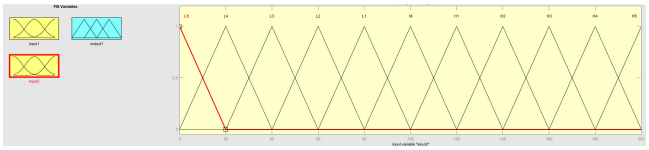

Fig. 6. Input 2 (actual voltage) membership functions.

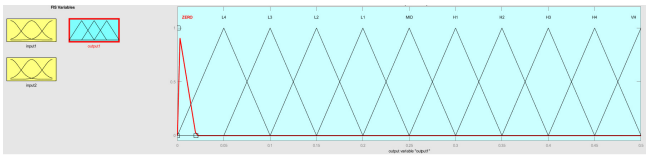

Fig. 7. De-fuzzified output (duty ratio output) membership functions.

TABLE III. FLC INPUT MFs AND RANGE

MF	Range of Voltage
L5	-20 to 20
L4	0 to 40
L3	20 to 60
L2	40 to 80
L1	60 to 100
M	80 to 120
H1	100 to 140
H2	120 to 160
H3	140 to 180
H4	160 to 200
H5	180 to 220

TABLE IV. FUZZY RULE BASE

		Input 1 MFs										
		L5	**L4**	**L3**	**L2**	**L1**	**M**	**H1**	**H2**	**H3**	**H4**	**H5**
Input 2 MFs	**L5**	ZER	ZER	ZER	ZER	ZER	ZER	ZER	ZER	ZER	ZER	ZER
	L4	L2	L3	L3	L4	L4	ZER	ZER	ZER	ZER	ZER	ZER
	L3	L2	L2	L2	L2	L4	L4	L4	L4	L4	L4	ZER
	L2	L1	L1	L1	L1	L2	L3	L4	L3	L4	L4	L4
	L1	MID	MID	L1	L1	L1	L1	L2	L2	L4	L3	L4
	M	H1	H1	H1	H1	H1	MID	L1	L1	L1	L2	L3
	H1	H1	H1	H1	H1	H1	H2	MID	L1	L1	L1	L2
	H2	H1	H1	H1	H1	H1	H2	H2	MID	MID	L1	L1
	H3	H2	H2	H1	H1	H1	H1	H1	H2	H1	MID	L1
	H4	H2	H2	H2	H2	H2	H2	H2	H2	H2	H1	MID
	H5	H2	H2	H2	H2	H2	H2	H2	H2	H2	H1	H1

VI. RESULTS AND DISCUSSION

The complete simulation schematics of the bridgeless dual Cuk converter controlled by the FLC are shown in Figure 8. As can be noted, the BDC Cuk converter has a significant advantage over the conventional bridge-type converters. The FLC converter performs efficiently with a fast response to inputs and gives good power quality indices. Figure 10 shows its output voltage response. As the FLC is mainly employed to improve power quality, the input side power quality parameters are very important.

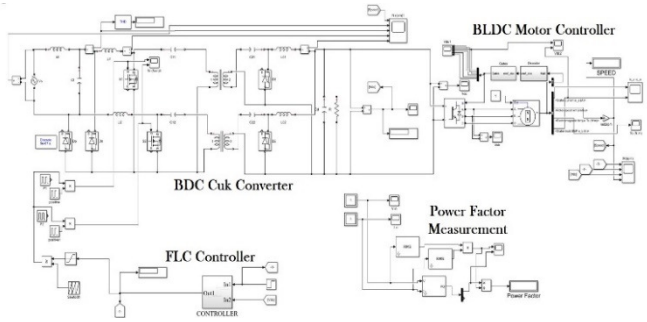

Fig. 8. Simulation diagram of the BDC converter with FLC.

Figure 9 shows the pure sinusoidal waveform of the supply current in the FLC-based converter compared to the partially sinusoidal current profile in the PID controller one.

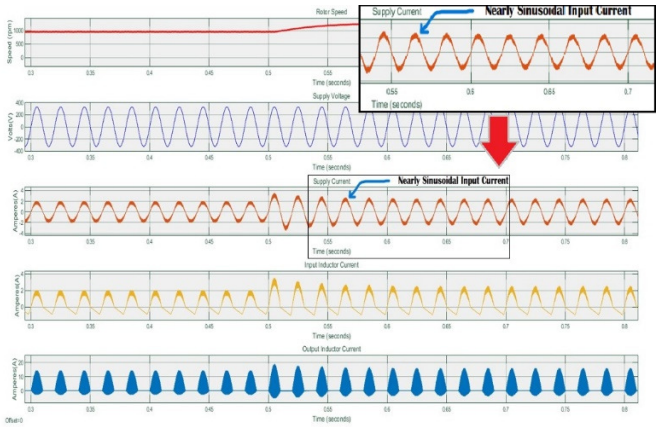

Fig. 9. Rotor speed, source voltage, source current, input inductor current, and output inductor current.

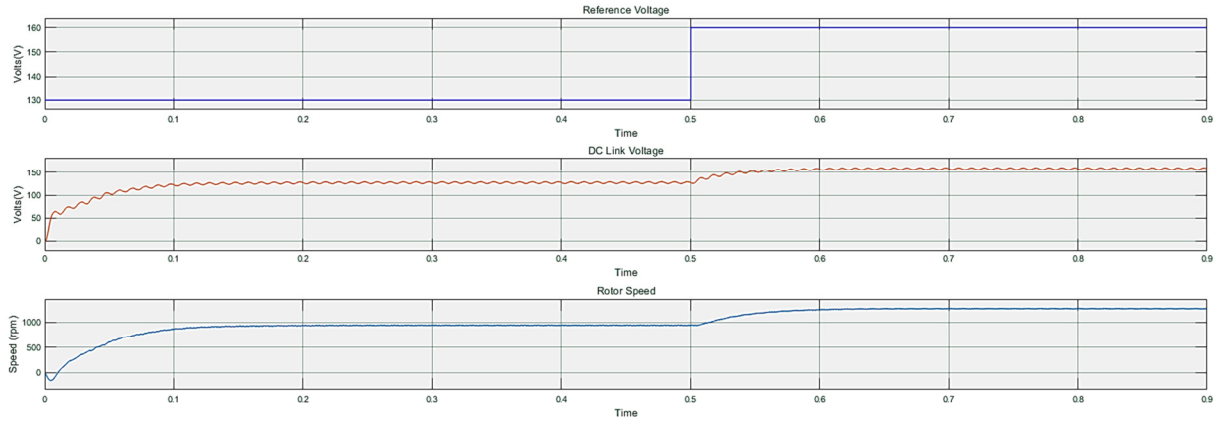

Fig. 10. Rotor speed output for the step reference voltage input.

A. *THD Analysis*

The harmonic content in the supply current can be determined by finding the THD value. This value was computed taking into account the percentage values of individual harmonic current components for the fundamental value. Also, some DC components may be present in the circuit due to switching losses or EMI, which should also be considered. By default, it was assumed to be 1%, unless it is present significantly. THD is the ratio of the root mean square sum of the individual harmonic components to the fundamental value. Either the percentile or the actual value of harmonics can be used. This study used harmonics as the percentage of the fundamental.

$$\text{THD}(\%)=\sqrt{\frac{(I_2{}^2+I_3{}^2+I_4{}^2+\ldots+I_n{}^2)}{I_1{}^2}}\times 100(\%)+\text{DC Component}(\%) \quad (13)$$

The DC component was not present in the harmonic analysis, so it was assumed to be 1%. From Table V we get:

$$\text{THD}(\%)=\sqrt{\frac{(3.2^2+1.2^2+0.8^2+0.6^2+0.3^2+0.2^2+0.15^2+0.1^2+0.15^2)}{100^2}}\times 100\ ($$

THD(%) was 4.58%, which is close to the simulated value (3.98%). The analysis of the THD content on the supply current, shown in Figure 11, shows that the BDC converter with advanced FLC significantly improved the power quality of the input supply. It can be noted that the THD levels significantly dropped to 3.98% compared to conventional converter topologies [10].

TABLE V. CURRENT HARMONICS IN BDC CONVERTER WITH FUZZY LOGIC CONTROLLER

Harmonic Order	Value (% of fundamental)
3	3.2
5	1.2
7	0.8
9	0.6
11	0.3
13	0.2
15	0.15
17	0.1
19	0.15
DC Component	1%

B. *Power Factor*

The BDC topology achieved a very high power factor, almost close to unity (0.99), compared to the other two conventional topologies with PFs of 0.95 and 0.97 respectively [10], as shown in Figure 12. Compared to conventional topologies, the proposed BDC scheme has the advantage of a

wide operating range because of the reduced stress on the operating components. Due to the single half-cycle specific operation of the converter, the BDC method used relatively fewer components at a time with minimal power rating.

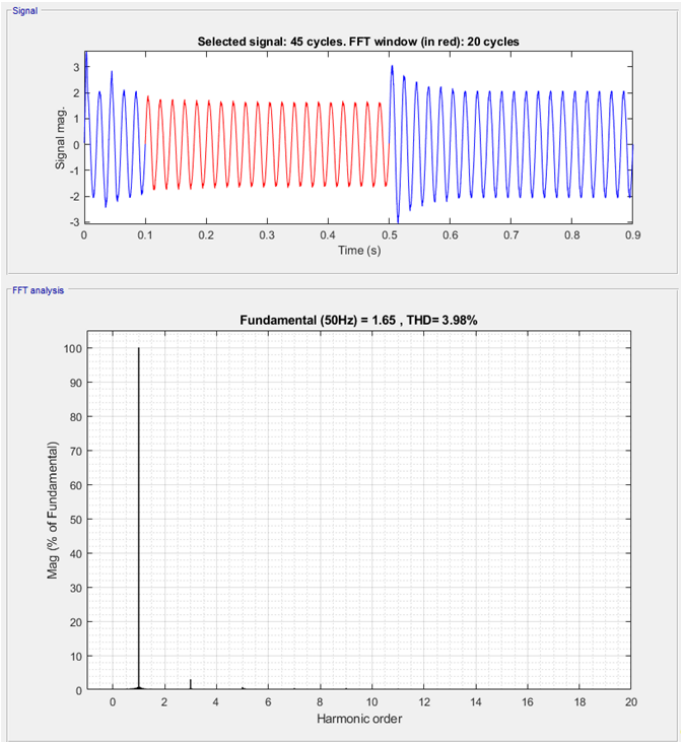

Fig. 11. THD analysis.

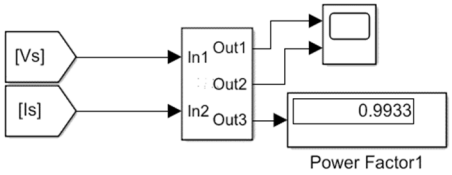

Fig. 12. Results of power factor analysis.

C. *Efficiency*

The performance of the three converters was examined to analyze their operation efficiency. As the VSI-fed BLDC motor part is the same for the three converters, the back end of the PFC converter was used to calculate the output power. Figure 13 shows that due to the absence of a current controller and the inherent conduction loss of the rectifier diodes, the overall efficiency was very low, ranging from 42.7% to an underwhelming 62.7%, even at the motor-rated voltage. The current multiplier method, due to the incorporation of the current controller and amidst the heavy conduction loss in the DBR, controlled the power loss and presented a much more efficient operation. The efficiency values were 51% at 40V DC and ranged to a maximum of 73.2% at the rated motor voltage of 200V DC. The proposed design rectified the issues of the previous topologies. The conduction loss is not a concern, as the DBR was eliminated, and the converter operation used a single sensor control for the same reason. The DCM operation resulted in a better power factor, and the power transfer was smooth due to the coupled configuration of the Cuk converter. The efficiency of the converter was in the range of 88.7-96.1% at the rated motor voltage. Moreover, the life of the switching components can be extended because of the reduced transient time when the converter switches are subjected to switching stress due to the single half-cycle operation of each converter.

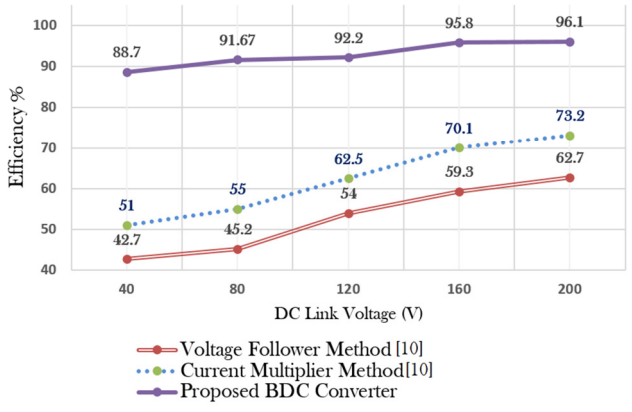

Fig. 13. Comparison of converter efficiency.

VII. CONCLUSION

The power quality of a new BLDC motor-based speed control drive was analyzed and the results showed that the proposed design attained significantly better power quality parameters compared to the conventional topologies [10]. The power factor and THD of conventional Cuk and proposed bridgeless dual Cuk converter topologies were analyzed using the simulated results for varying input conditions. The proposed method was portrayed to assert the merits of the BDC converter in attaining a power factor nearly unity for the drive. The fuzzy logic controller-based control strategy of the converter enhanced the performance of the modified Cuk converter and helped to achieve a very low THD value. The method was simulated using Matlab 2018 based on varying input conditions. The analysis proved experimentally that the BDC design was more efficient and the FLC-based BDC converter was the most efficient among other topologies and is suitable for modern variable speed electric drives that employ BLDC motors. The reduction of current sensors, one-cycle operation, and low current stress on the power electronic switches make it suitable for long-duration operation. Therefore, this topology is a notable choice for high-power motor drive schemes used in household and industrial equipment.

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