An MPPT-based 31-Level ADC Controlled Micro-Inverter

Maulik J. Shah
Department of Electrical Engineering, CSPIT, CHARUSAT
Charotar University of Science and Technology
(CHARUSAT), CHARUSAT Campus
Changa, Gujarat, India
maulikniki@gmail.com

Kartik S. Pandya
Department of Electrical Engineering, CSPIT, CHARUSAT
Charotar University of Science and Technology
(CHARUSAT), CHARUSAT Campus
Changa, Gujarat, India
kartikpandya.ee@charusat.ac.in

Priyesh Chauhan
Electrical and Computer Science Engineering
Institute of Infrastructure, Technology, Research and Management
Gujarat, India
priyeshchauhan@iitram.ac.in

Received: 12 July 2022 | Revised: 22 July 2022 | Accepted: 24 July 2022

Abstract-This paper presents a 31-level micro-inverter with an innovative control scheme. The presented micro-inverter makes use of a single PV panel connected to an MPPT converter. Four half-bridge legs are connected in series to produce 31 levels at the inverter's output. At the output side of the micro-inverter, a single full-bridge power circuit is used to generate positive and negative half-cycles. A high-frequency transformer and a push-pull converter are used to generate the required isolated DC sources. The output of an Analog to Digital Converter (ADC) is used as a gate pulse for the half-bridge circuit power switching devices. PSIM software was used to simulate the proposed micro-inverter, and the results are discussed. Hardware prototypes were also created and the results are displayed.

Keywords-analog to digital converter; micro-inverter; MPPT; PV panel; Perturb and Observe

I. INTRODUCTION

A solar micro-inverter, also known as a micro-inverter, is a plug-and-play photovoltaic's component that transforms the Direct Current (DC) produced by a single solar module into Alternating **C**urrent (AC). Micro-inverters stand in contrast to traditional string and central solar inverters, which connect a single inverter to several solar panels. The output of multiple micro-inverters can be pooled and often sent into the power grid. Compared to normal inverters, micro-inverters provide several benefits. The key benefit is that they electrically isolate the panels from one another, so even a full module failure or minor quantities of shade, dust, or snow lines on one solar module do not significantly diminish the output of the entire array. By conducting Maximum Power Point Tracking (MPPT) for the modules it is attached to, each micro-inverter collects the most power possible. Since each inverter must be put next to a panel, one of the main drawbacks of a micro-inverter is that it has a greater initial equipment cost per peak Watt than a central inverter of similar power (usually on a roof). Due to this, they are also more difficult to maintain and expensive to take apart and replace. In this proposed MPPT-based 31-level micro-inverter, the multi-level inverter is used to reduce the harmonics at the output. Figure 1 shows the basic block structure of the proposed micro-inverter.

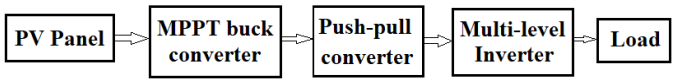

Fig. 1. Basic block structure of the proposed system.

There are many MPPT techniques available. Two common types are: conventional algorithms and intelligent control algorithms [1, 3]. In [1], a different comparative analysis of MPPT algorithms is presented. This paper simulated a 100kW grid-connected PV system with a beta control algorithm. Based on the previously known value, the accuracy of MPPT can be improved [7]. In the proposed inverter, the PV panel is used for MPPT with the Perturb and Observe (P&O) algorithm. A push-pull converter is used to separate a single source into many isolated DC sources. It employs a high-frequency transformer with a primary winding with a center tap and four different secondary windings. The isolated sources are used as asymmetric DC sources for the Multi-Level Inverter (MLI). Many MLI topologies are used nowadays to reduce the output voltage Total Harmonic Distortion (THD). Optimized topologies for MLI are represented in [2] with asymmetric and symmetric DC sources. The home type cascaded MLI with reduced power switching devices is presented in [4]. The asymmetric MLI gives higher output voltage levels than symmetric MLIs [5]. In the proposed topology, asymmetric power configuration is used for the generation of the 31-level output and a direct ADC control scheme is developed for the

Corresponding author: Maulik J. Shah

inverter to get a 31-level output voltage. In this scheme, the output of the ADC is directly used as gate pulses of power switching devices in half-bridges.

II. MODELING OF THE PV MODULE

The equivalent circuit model for the PV module is shown in Figure 2. The equivalent circuit includes a current source in parallel with a diode and resistance. I_{ph} is the photo current, I_D is the diode current, R_{sh} and R_s show the shunt resistance and series resistance respectively [1, 3].

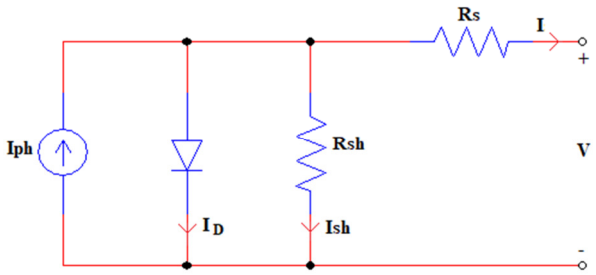

Fig. 2. Equivalent circuit for the PV cell.

$$I = I_{ph} - I_S\left(\exp\left(\frac{qV+qR_sI}{NKT}\right) - 1\right) - \left(\frac{V+R_sI}{R_{sh}}\right) \quad (1)$$

where I is the load current, I_s the diode saturation current, and T is the cell temperature.

$$V = I_{ph}R_{sh} - IR_{sh} + I_S\left(\exp\left(\frac{qV+qR_sI}{NKT}\right) - 1\right) - IR_s \quad (2)$$

By modifying (1), we get:

$$V = I_{ph} - I_S\left(\exp\left(\frac{qV+qR_sI}{NKT}\right) - 1\right) - \frac{V}{R_{sh}} - \frac{R_sI}{R_{sh}} \quad (3)$$

$$I + \frac{R_sI}{R_{sh}} + I_S\left(\exp\left(\frac{qV+qR_sI}{NKT}\right)\right) = I_s - \frac{V}{R_{sh}} + I_{ph} \quad (4)$$

From (4) we will get:

$$\left(\frac{R_s+R_{sh}}{R_{sh}I_s}\right)I + \left(\exp\left(\frac{qV}{NKT}\right) \times \exp\left(\frac{R_sI}{NKT}\right)\right) = 1 - \frac{V}{R_{sh}I_s} + \frac{I_{ph}}{I_s} \quad (5)$$

An analytical solution for (5) is not possible. So, we ignore parameter Rs and thus we get:

$$I = \frac{1}{\left(\frac{R_{sh}}{R_{sh}I_S}\right)} - \left(1 - \frac{V}{R_{sh}I_S}\right) - \left(\exp\left(\frac{qV}{NKT}\right)\right) + \frac{I_{ph}}{I_s} \quad (6)$$

A. Maximum Power Point Tracking

MPPT is a method for maximizing energy extraction from variable power sources as conditions change. The main issue that MPPT attempts to solve is the fact that the efficiency of power transmission from the solar cell is dependent on the quantity of sunlight, the amount of shade, the temperature of the solar panel, and the electrical characteristics of the load. The load characteristic (impedance) that provides the maximum power transmission changes when these variables change. The system is optimized in order to maintain the best efficiency of power transfer as the load characteristic changes. The Maximum Power Point (MPP) refers to this ideal load property. Any enhancement to the MPPT's rise time will raise the system's efficiency and power extraction while also increasing system reliability. There are many algorithms developed for MPPT, such as the P&O algorithm, the incremental conductance, and ripple correlation

B. Perturb and Observe (P&O)

By adjusting the voltage from the array by a little amount, the controller measures the power and, if it rises, tries more adjustments in that direction until the power stops rising. P&O is the most popular strategy because it is very simple to use, although it might lead to oscillations in the power output. Because it depends on the increase of the power versus voltage curve below the MPP and the decrease above that point, it is also known as the "hill climbing" approach. If a suitable predictive and adaptive hill climbing strategy is used, P&O method may produce top-level efficiency [1].

III. INVERTER WITH DIRECT ADC CONTROL SCHEME

All supplied DC sources in symmetric MLIs have the same magnitude, however in asymmetric MLIs, the magnitude of the supplied DC sources varies. DC sources are employed in asymmetric MLI binary or trinary types. DC sources in the binary pattern include Vdc, 2Vdc, 4Vdc, etc. DC sources of the trinary kind include Vdc, 3Vdc, 9Vdc, etc. However, the control strategy is quite complicated in trinary type power topologies and calls for a look-up table for switching power devices. Using an analog to digital conversion IC or an ADC channel built into a processor or microcontroller chip, the reference signal in binary-type DC sources can be converted directly. Using 4 isolated DC sources, an inverter with a total of 12 power switching components and 6 half-bridge MOSFET/IGBT driver circuits may provide an output voltage with 31 levels.

A. Direct ADC Control Scheme

There is no need for a triangular carrier wave in the direct ADC-controlled method. It produces n-bit controlled signals based on a look-up table for the sine wave's first half cycle. The resulting signals are immediately applied to the half-bridge of the inverter's gate pulses. As switching losses are reduced, an inverter's total efficiency also rises since the direct ADC method's switching frequency is lower than that of all PWM systems. The creation of gate pulses depends on the bit resolution of the ADC. The number of levels of the output voltage of the MLI is determined by the bit resolution of the ADC in this control system. As with 2-bit resolution, this will make only $(2*2^2)$-1=7 level output, a 3-bit resolution will make $(2*2^3)$-1=15 level output, and 4-bit will give $(2*2^4)$-1 = 31 levels.

IV. SIMULATIONS AND RESULTS

The simulation validation of the proposed micro-inverter topology was carried out in PSIM software. Figure 3 shows a complete simulated block diagram of the micro-inverter. A simulated block diagram contains a total of 3 subsystems and 1 PV panel. The MPPT converter is developed in the first sub-system S1. Subsystem S2 contains a push-pull converter with a high-frequency converter, and S3 includes a 31-level micro-inverter system.

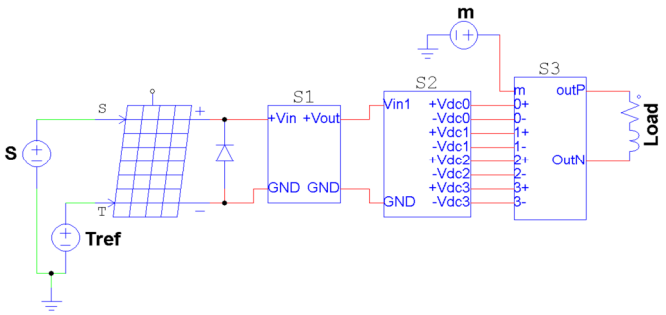

Fig. 3. Block diagram of the simulated system in PSIM.

A. PV panel and MPPT Converter

ASP-7-330 (Adani) PV panel was used for simulation in PSIM. Its specifications are given in Table I at 1000W/m² irradiance and 25°C cell temperature. In the simulation of the full system, the P&O algorithm is used for MPPT.

TABLE I. PV PANEL SPECIFICATIONS

Parameters	Value
Peak power (Pmax)	330W
Maximum Voltage (Vmpp)	37.21V
Maximum current (Impp)	8.87A
Open circuit voltage (Voc)	45.87V
Short circuit current (Isc)	9.42A
Module efficiency	16.84%

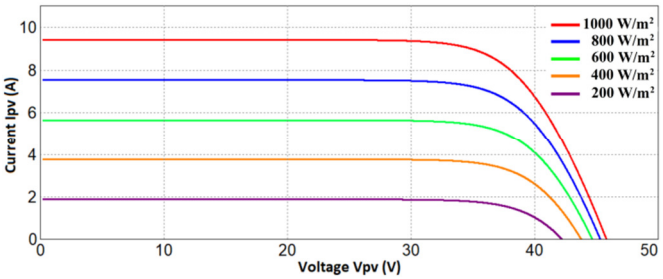

Fig. 4. I-V characteristics of the PV panel at 25°C at different irradiances.

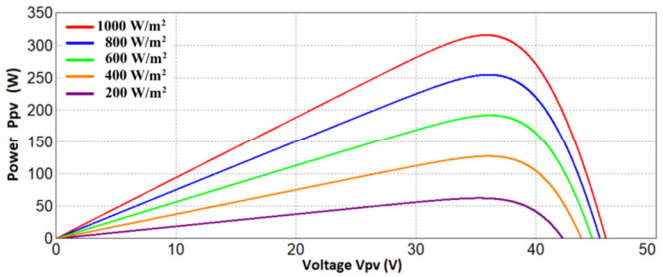

Fig. 5. P-V characteristics of the PV panel at 25°C at different irradiances.

Figures 4 and 5 show the obtained I-V and P-V characteristics at 25°C and at different irradiances: 200W/m^2 to 1000W/m^2 irradiance is taken at 25°C for I-V and P-V characteristics of the PV panel. Figure 6 represents the complete MPPT buck converter connected with PV panel. In this +Vin is coming from the positive terminal and GND is coming from the negative terminal of the PV panel. In MPPT block the P&O algorithm was developed in C language with the inputs the supply voltage (Vin) and current (I) of the PV panel. The switching frequency of the PWM pulse is 20kHz.

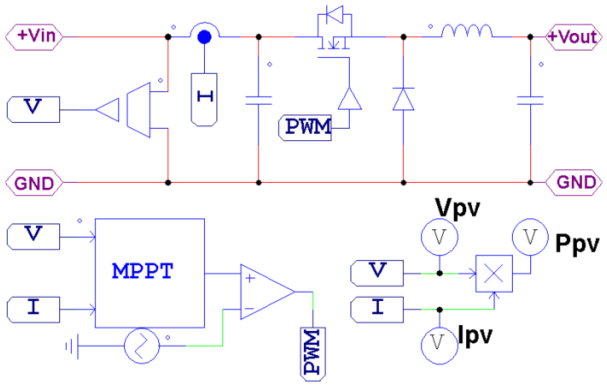

Fig. 6. Simulation diagram of the MPPT buck converter.

B. Push-Pull Converter with High-Frequency Transformer

The output of the MPPT converter +Vout and GND is connected to the supply of the push-pull converter. The push-pull converter is used to create isolated DC sources from a single source. It uses a high-frequency transformer with center tap primary winding and four numbers of secondary windings. Secondary winding turns are chosen such that it gives binary types of supply voltages like 12, 24, 48, and 96V. Each secondary winding is connected with a full-bridge diode rectifier to convert AC power into DC power. Each output is used as a power supply of the inverter half-bridges. Figure 8 shows the push-pull converter with a high-frequency transformer. Vdc0, Vdc1, Vdc2, and Vdc3 created the isolated DC sources in Figure 7. Figure 8 shows the output of the push-pull converter.

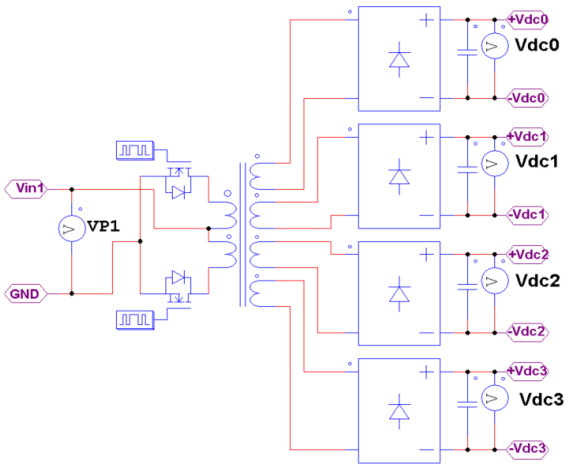

Fig. 7. Push-pull converter to create isolated DC sources.

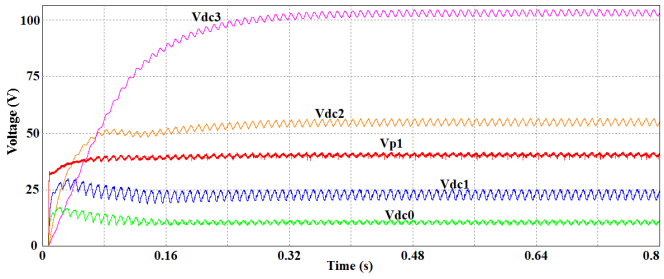

Fig. 8. Simulated output of the push-pull converter.

C. The 31-Level Inverter

One half-bridge circuit of the power switching device is connected to each DC source that is created by the push-pull converter. To generate the negative and positive cycle, one full-bridge circuit is employed. The full-bridge circuit's gate pulse is generated by the zero-crossing logic's output. Therefore, this H-switching bridge's frequency is comparable to its power frequency. The gate pulses of power switches S0 and S01 are working in inverting mode. Gate driver IC is used to generate the dead band in the gate pulses of these two switches. For S1-S11, S2-S21, S3-S31, and Sh1-Sh11, Sh2-Sh21, the same reasoning is used. Assuming Vdc0 = 12V, Vdc1 = 24V, Vdc2 = 48V, and Vdc3 = 96V would follow. The power structure for the proposed 31-level inverter is shown in Figure 9.

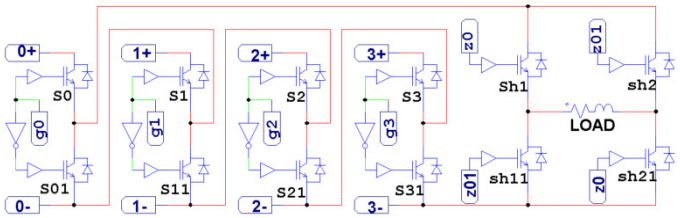

Fig. 9. Simulated power circuit of the 31-level inverter.

Switching appears to take the form of a binary conversation. Therefore, all DC sources are connected in series for the +15 Vdc output level. In the 4-bit binary, it is simply $(1111)_2$, which represents the states of power switches S3, S2, S1, and S0 respectively. Similar to the +10 Vdc case, the states are $(1010)_2$ in binary, meaning that switches S3 and S1 are in the on position, while S2 and S0 are in the off position. Figure 10(a) shows the simulated output voltage of the micro-inverter with a load of 65Ω connected in series with a 63.7mH inductor at modulation index 1.0. Figure 10(b) shows the zoomed view of the output voltage and Figure 11 shows the load current of the inverter. Figure 12 shows a comparison between the output voltage of the inverter and the grid voltage.

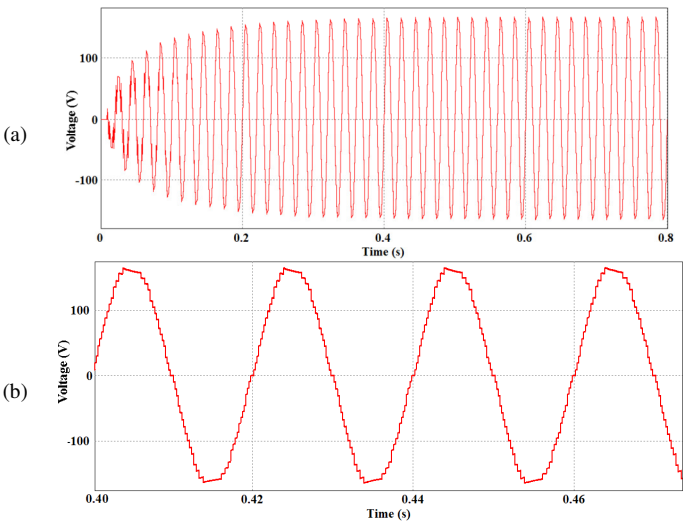

Fig. 10. (a) Output Voltage at R=65Ω and L=63.7mH at modulation index m=1.0, (b) zoomed view of the output voltage.

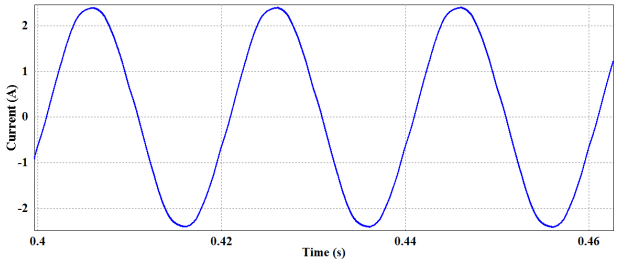

Fig. 11. Load current at R=65 Ω and L=63.7mH at m=1.0.

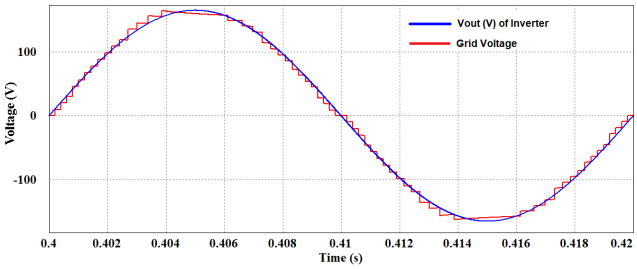

Fig. 12. Compared output Voltage of the inverter and grid voltage.

TABLE II. THD OF THE OUTPUT VOLTAGE AND LOAD CURRENT AT DIFFERENT MODULATION INDEX VALUES

Modulation Index (m)	THD (%)	
	Voltage (Vout)	Current (Iout)
1.0	3.16	0.82
0.9	3.67	1.23
0.8	3.93	1.12
0.7	4.95	1.67
0.6	5.40	1.76
0.5	6.42	1.69

Table II shows the % THD of the output voltage and load current concerning the fundamental components. It can be seen that THD will increase with the decrease in the modulation index value. As the modulation index is decreasing, the number of levels at the output side of the inverter decreases.

V. HARDWARE RESULTS

For the testing of the ADC control scheme, a hardware prototype of the inverter with isolated DC sources was developed. Each half-bridge MOSFET is driven by an IR 2104 half-bridge driver IC. So, the proposed MLI uses a total of 6 IR2104 driver ICs. A built-in dead-band facility exists between the top and lower MOSFETs of the IR2104 driver IC. Therefore, a dead band between two inverted gate pulses can be generated without the need for any additional hardware or software. For the 4 half-bridge circuits, IRFB4110 MOSFETs were used as power switching devices, and IRFP460N MOSFETs for full h-bridge circuits. To protect the microcontroller, 817 opto-coupler IC was used to isolate the gate pulses from the microcontroller. The hardware prototype was tested on resistive and inductive loads. Figure 13 shows the output of ADC that is used as gate pulses for four half-bridges. Figures 14 and 15 show the output voltage of an inverter at m=1.0 and m=0.8 respectively. Figure 16 shows the inverter output voltage in comparison with the grid voltage.

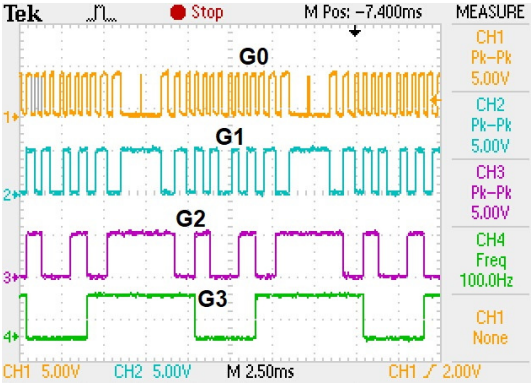

Fig. 13. Gate Pulses generated using ADC

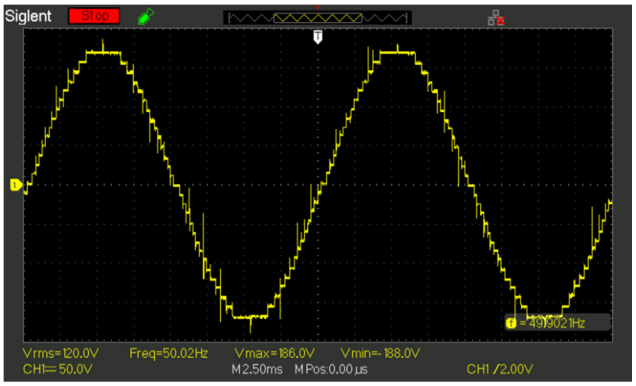

Fig. 14. Inverter output voltage at modulation index m=1.0.

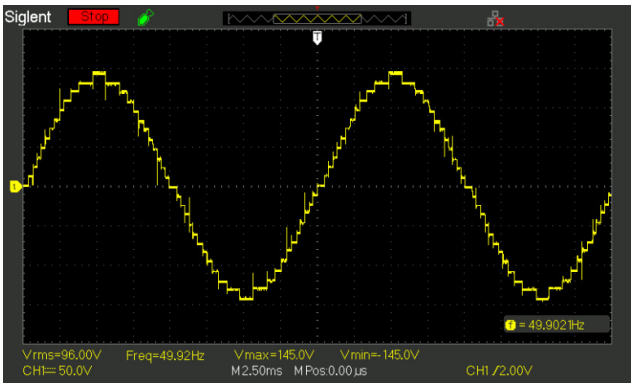

Fig. 15. Inverter output voltage at m=0.8.

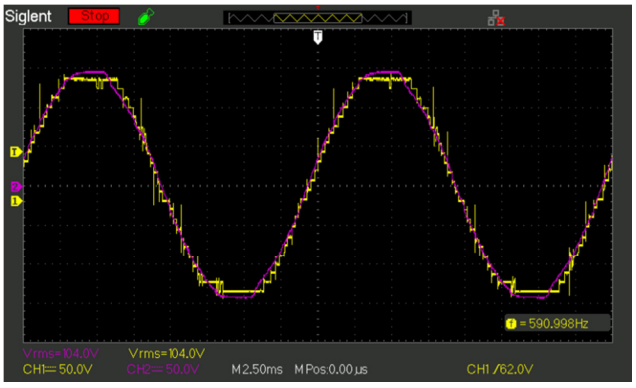

Fig. 16. Inverter output voltage in comparision with the grid voltage. (yellow color: inverter output, purple color: grid voltage).

VI. CONCLUSION

In the proposed topology of the micro-inverter, the number of necessary DC power sources is reduced by using binary level DC sources. The inverter output voltage reached 31 levels utilizing only 4 isolated DC sources and direct ADC control. At modulation index m=1, the THD of the inverter output voltage was reduced to 2.11%. When compared to other control methods like SPWM, SVPWM, etc. the direct ADC control scheme utilized in this study is quite straightforward. Here, there is no need to contrast any carrier (triangular) wave with the reference sine wave. The direct ADC control approach makes it simple to create a grid connection for an inverter. The proposed MLI's RMS output voltage will fluctuate in line with variations in the grid's RMS voltage. The fundamental benefit of this control strategy is that the frequency of the grid and the output voltage are constantly synchronized.

REFERENCES

[1] F. Z. Kebbab, L. Sabah, and H. Nouri, "A Comparative Analysis of MPPT Techniques for Grid Connected PVs," *Engineering, Technology & Applied Science Research*, vol. 12, no. 2, pp. 8228–8235, Apr. 2022, https://doi.org/10.48084/etasr.4704.

[2] B. M. Manjunatha, S. N. Rao, A. S. Kumar, K. S. Zabeen, S. Lakshminarayanan, and A. V. Reddy, "An Optimized Multilevel Inverter Topology with Symmetrical and Asymmetrical DC Sources for Sustainable Energy Applications," *Engineering, Technology & Applied Science Research*, vol. 10, no. 3, pp. 5719–5723, Jun. 2020, https://doi.org/10.48084/etasr.3509.

[3] M. T. Ahmed, M. R. Rashel, F. Faisal, and M. Tlemcani, "Non-iterative MPPT Method: A Comparative Study," *International Journal of Renewable Energy Research*, vol. 10, vo. 2, pp. 549–557, Jun. 2020.

[4] P. L. Kamani and M. A. Mulla, "A Home-type (H-type) Cascaded Multilevel Inverter with Reduced Device Count: Analysis and Implementation," *Electric Power Components and Systems*, vol. 47, no. 19–20, pp. 1691–1704, Dec. 2019, https://doi.org/10.1080/15325008.2019.1660735.

[5] M. Farhadi Kangarlu and E. Babaei, "Cross-switched multilevel inverter: an innovative topology," *IET Power Electronics*, vol. 6, no. 4, pp. 642–651, 2013, https://doi.org/10.1049/iet-pel.2012.0265.

[6] D. Shunmugham Vanaja and A. A. Stonier, "A novel PV fed asymmetric multilevel inverter with reduced THD for a grid-connected system," *International Transactions on Electrical Energy Systems*, vol. 30, no. 4, 2020, Αρτ. No. e12267, https://doi.org/10.1002/2050-7038.12267.

[7] M. Chellal, T. F. Guimarães, and V. Leite, "Experimental Evaluation of MPPT algorithms: A Comparative Study," *International Journal of Renewable Energy Research (IJRER)*, vol. 11, no. 1, pp. 486–494, Mar. 2021.

[8] V. Pakala and S. Vijayan, "A New DC-AC Multilevel Converter with Reduced Device Count," *International Journal of Intelligent Engineering and Systems*, vol. 10, no. 3, pp. 391–400, Jun. 2017, https://doi.org/10.22266/ijies2017.0630.44.

[9] P. Manoharan, S. Rameshkumar, and S. Ravichandran, "Modelling and Implementation of Cascaded Multilevel Inverter as Solar PV Based Microinverter Using FPGA," *International Journal of Intelligent Engineering and Systems*, vol. 11, no. 2, pp. 18–27, Apr. 2018, https://doi.org/10.22266/ijies2018.0430.03.

[10] M. Jagabar Sathik, N. Prabaharan, S. a. a. Ibrahim, K. Vijaykumar, and F. Blaabjerg, "A new generalized switched diode multilevel inverter topology with reduced switch count and voltage on switches," *International Journal of Circuit Theory and Applications*, vol. 48, no. 4, pp. 619–637, 2020, https://doi.org/10.1002/cta.2732.

[11] D. A. Tuan, P. Vu, and N. V. Lien, "Design and Control of a Three-Phase T-Type Inverter using Reverse-Blocking IGBTs," *Engineering, Technology & Applied Science Research*, vol. 11, no. 1, pp. 6614–6619, Feb. 2021, https://doi.org/10.48084/etasr.3954.

[12] J. Chakravorty and G. Sharma, "DVR with Modified Y Source Inverter and MCFC," *Engineering, Technology & Applied Science Research*, vol. 9, no. 1, pp. 3803–3806, Feb. 2019, https://doi.org/10.48084/etasr.2522.

[13] S. Paul, P. Jacob, and J. Jacob, "Performance Comparison of Stand Alone Solar PV System with Variable Step Size MPPT," *International Journal of Renewable Energy Research (IJRER)*, vol. 10, no. 3, pp. 1277–1286, Sep. 2020, https://doi.org/10.20508/ijrer.v10i3.11212.g8002.

[14] Z. Boumous and S. Boumous, "New Approach in the Fault Tolerant Control of Three-Phase Inverter Fed Induction Motor," *Engineering, Technology & Applied Science Research*, vol. 10, no. 6, pp. 6504–6509, Dec. 2020, https://doi.org/10.48084/etasr.3898.

[15] U. B. Tayab and M. A. A. Humayun, "Modeling and Analysis of a Cascaded Battery-Boost Multilevel Inverter Using Different Switching Angle Arrangement Techniques," *Engineering, Technology & Applied Science Research*, vol. 7, no. 2, pp. 1450–1454, Apr. 2017, https://doi.org/10.48084/etasr.1094.