Direct ADC Controlled Asymmetric Cascaded Multilevel Inverter

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Abstract-This paper presents an asymmetric multi-level inverter with a novel direct ADC control scheme. This scheme does not use a carrier wave or a reference sinusoidal wave to generate gate pulses for power switches, but an Analog to Digital Converter (ADC) to create gate pulses. For n sources, n bit ADC will generate 2^{n+1}-1 levels at the output voltage of the inverter. This scheme uses the ADC output for the gate pulses for power switching devices. In this topology, the inverter comprises a series of connected half-bridges to generate a more significant level. The presented topology uses binary level supply voltages. Different topologies with different parameters are compared with the proposed inverter, and the operation of the proposed control scheme is verified with a simulation in Matlab. The prototype of a 31-level inverter is developed in hardware, and the hardware results are discussed.

Keywords-analog to digital converter; cascaded inverter; reduced power switching devices; multilevel inverter

I. INTRODUCTION

For less Total Harmonic Distortion (THD) in the output voltage of an inverter, in medium power applications, multilevel inverters (MLIs) are most preferred. MLIs have become very popular due to their power topologies. They are widely used for medium voltage applications like grid-connected inverters, traction systems, and FACTS.

The current paper presents enormous topologies and their control switching pattern [1]. MLIs are classified into two categories, symmetric and asymmetric, based on their supply DC sources [5]. Here, the proposed topology is asymmetric as supplied DC voltages are different in magnitude. Simulated and hardware prototypes of four DC voltage sources were used. Four half-bridges were connected in series in a power circuit, and the series' output was connected to one full-bridge inverter. A novel finite predictive control method was described in [2]. A three-phase inverter asymmetric fault-tolerant control scheme was illustrated in [3] to limit the fault phase's fault current. Using diode rectifiers, isolated DC-DC converters were implemented to reduce the power switching devices in [4]. A home-type cascaded inverter was presented in [6]. The authors used unidirectional and bi-directional switches in the power circuit. Without any additional structure like H-bridges, the given topology can generate a uniform positive and negative cycle at the output of the MLI. The limitation of this topology is that it requires bidirectional switches. Matlab simulation of T-type 3 level inverter is represented in [7] for the field oriented control of traction motor. PMSM motor control using multi-level inverter with active damping and current controller was described in [8].

II. POWER CIRCUIT AND OPERATION

Based on the amplitude of the supplied DC voltage sources, output voltage levels can be adjusted. MLI can be classified into two categories, depending on the DC sources: Symmetric and asymmetric. In symmetric MLI, all the supplied DC sources are equal in magnitude, while in asymmetric, the magnitudes of the supplied DC sources are different. In asymmetric MLI, binary or trinary type DC sources are used. In the binary pattern, DC sources are, for example, Vdc, 2Vdc, 4Vdc, etc. In trinary type, DC sources are like Vdc, 3Vdc, 9Vdc, etc. However, in trinary type power topologies, the control scheme is somewhat complex and requires a look-up table for switching power devices. In binary type DC sources, the reference signal can be converted directly in binary form using analog to digital conversion IC or onboard an ADC channel of processor or micro-controller chip. In some processors, such as the ARM series, floating-point ADC is available and can also give negative signals. If floating-point

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ADC is unavailable, then the Vref signal is converted first in absolute value.

For n isolated binary level DC sources:

- The number of levels achieved at an output voltage of an inverter is 2^{n+1}-1
- The number of power switching devices required is (2*n) + 4
- The number of gate drivers (half-bridge driver) required is n + 2

From the above, if we use four isolated DC sources, one can achieve a 31-level output voltage of an inverter with a total of 12 power switching devices and 6 half-bridge MOSFET / IGBT driver circuits.

In the proposed ADC-controlled MLI, binary-type DC sources are used, e.g. 12V, 24V, 48V, and 96V. All the DC sources are connected to one half-bridge circuit of the power switching device. So, 4 half-bridge circuits are used, and 1 full-bridge circuit generates the negative and positive cycle. The output of zero-crossing logic is used as a gate pulse for the full-bridge circuit. So, the switching frequency of this full H-bridge is similar to the power frequency. Gate pulses for S0 and S01 power switches are operating in inverting mode. So, in the gate pulses of these 2 switches, the dead band is generated using driver IC. Similar logic is also applied for S1-S11, S2-S21, S3-S31, and Sh1-Sh11, Sh2-Sh21. Suppose Vdc0 = Vdc, then Vdc1 = 2*Vdc, Vdc2 = 4*Vdc, and Vdc3 = 8*Vdc. Figure 1 shows the power topology for the proposed 31-level MLI. Table I shows the switching pattern for 31 levels. It is seen that switching is done like a binary conversation. So, for the +15 Vdc output level, all DC sources are connected in series. So, this is nothing but $(1111)_2$ in 4-bit binary, indicating the states of power switches S3, S2, S1, and S0 respectively. Similarly, for +10 Vdc the states are $(1010)_2$ in binary, which means switches S3 and S1 are in on state, and S2 and S0 are in off state.

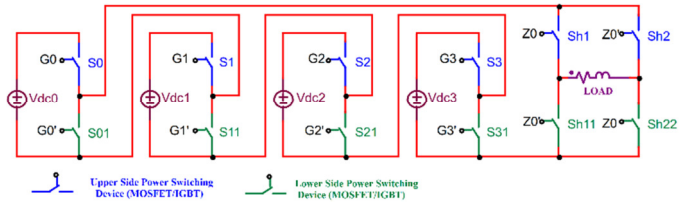


Fig. 1. Power topology of the 31-level MLI.

TABLE I. SWITCHING STATES OF THE 31-LEVEL INVERTER

S3	S2	S1	S0	Sh1	Sh2	Output
1	1	1	1	1	0	+15 Vdc
1	1	1	0	1	0	+14 Vdc
⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	0	1	1	0	+1 Vdc
0	0	0	0	1	0	0 Vdc
0	0	0	1	0	1	-1 Vdc
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	1	-15 Vdc

A. *Applications of the Proposed Inverter*

The proposed control scheme is straightforward to implement in a grid-tied inverter. This scheme is also applicable to a solar Micro-Inverter, and isolated DC sources can be implemented using a high-frequency transformer. It can also be applied for the speed control of an induction motor. Especially in electric vehicle systems, this inverter can be used where isolated DC sources are available in the form of batteries.

III. DIRECT ADC-BASED CONTROL SCHEME

Various topologies have been invented to reduce the harmonics in the output voltage of the MLI. Different techniques are available to control amplitude, frequency, and maintain a nearly sinusoidal waveform at the output of an MLI. The Selective Harmonic Elimination (SHE) method uses optimization techniques like PSO algorithm [11], Pulse Width Modulation (PWM), HPWM (Hybrid PWM), SPWM (Sinusoidal PWM), PRSPWM (Prior Switching PWM), SVPWM (Space Vector PWM), etc. In the SPWM technique, the sine wave is compared with high-frequency carrier waves, increasing switching losses. The arrangement of a triangular (carrier) wave in a different pattern is also needed, i.e. APOD (Alternate Phase Opposition Disposition), PD (Phase Disposition), POD (Phase Opposition Disposition). The direct ADC-controlled technique does not require any triangular carrier wave. Based on the look-up table of the first half cycle of the sine wave, it generates n-bit controlled signals. The generated signals are directly used as the gate pulses of the half-bridge of the inverter. In the direct ADC method, the switching frequency is less than in all the PWM methods, so the overall efficiency of an inverter increases as switching losses decrease.

The bit resolution of the ADC is essential for the generation of gate pulses. In this control scheme, the bit resolution of the ADC decides the number of levels of the output voltage of the MLI. As with 2-bit resolution, this will make only a $(2*2^2)$-1=7 level output, a 3-bit resolution will make a $(2*2^3)$-1=15 level output, and a 4-bit will give $(2*2^4)$-1=31 levels. As the number of resolutions increases, the required number of isolated DC sources also increases, which is the disadvantage of the proposed control scheme.

In the grid-connected inverter, the proposed control method is straightforward to control an inverter's output. When the grid voltage RMS value reduces, ADC conversion automatically changes, and the output of the inverter also reduces. Similarly, when there is a change in the supply frequency of the grid, the inverter output frequency also changes, which is the main advantage of the proposed MLI.

In this control method, the output of an MLI always remains in synchronization with the grid voltage. In the proposed technique, the inverter is always connected to the grid at a unity power factor, and DC link utilization is also full in. In all grid-connected topologies, a PLL block is required to synchronize the grid voltage with the inverter voltage. However, the proposed technique does not require a PLL block. In the current paper, a 4-bit control scheme is implemented in hardware. The prototype MLI is connected to

the grid to check the synchronization between the voltage of the grid and the inverter output voltage. Figure 2 shows the block diagram of the gate pulse generation through direct ADC.

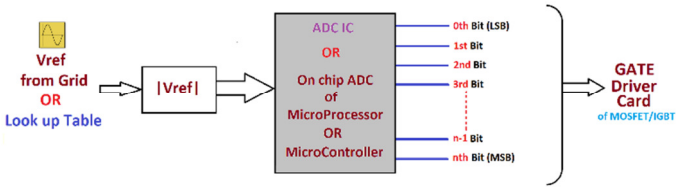


Fig. 2. ADC control block diagram of the MLI.

IV. COMPARISON WITH OTHER TOPOLOGIES

The following parameters are affected for properly evaluating different MLI topologies.

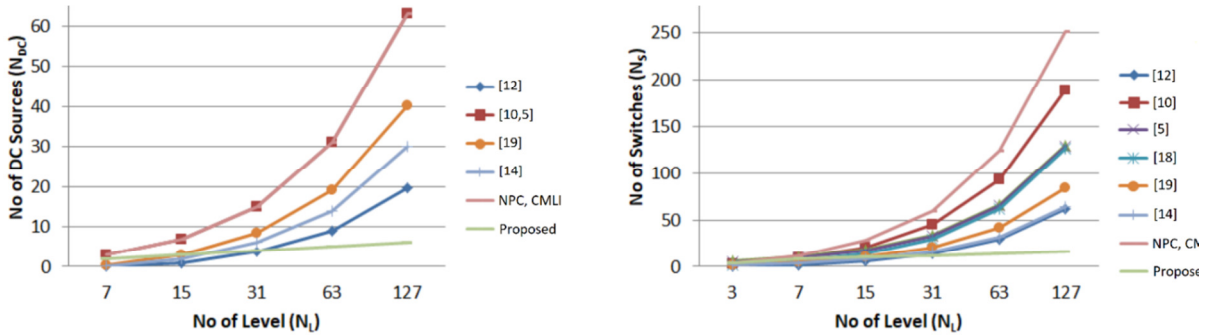
- Reliability and total cost
- Efficiency
- Performance, control schemes, and applications
- Dynamic response

The reliability and the cost of the inverter generally depend on the required number of power switches, the total blocking voltage capacity of that switching device, and the required DC sources (NDC). The efficiency of the inverter depends on the total number of power switching devices (NS), its blocking voltage capacity, and the switching frequency of the devices. Performance, control, and dynamic response of an inverter depend on power distribution, module structure, and the number of passive components.

TABLE II. SWITCHING STATES OF THE 31-LEVEL INVERTER

Ref. No.	N_L	N_S	N_{Driver}	N_{DC}	R
NPC	31	60	60	1	1.935
CHB	31	60	60	15	1.935
FC	31	60	60	1	1.935
14	31	16	12	6	0.516
17	31	10	10	5	0.322
18	33	28	28	8	0.903
19	17	12	12	5	0.387
20	31	12	12	4	0.387
Proposed	31	12	12	4	0.3871

So the proposed topology is compared with other 31-level inverters. Comparison is done considering the inverter output levels (N_L), the number of switching devices used (N_S), the total number of gate driver circuits (N_{Driver}), and the required DC sources (NDC). Table II compares the various known MLIs with the proposed 31-level inverter. The ratio (R) of switches to output level is also calculated. Topologies with a lower ratio are better than the ones with higher. From Table II, it can be seen that the proposed inverter uses fewer switches compared to other topologies. Figure 3 shows the comparison graph between the number of the required DC sources and the required number of power switching devices respectively. From all comparison graphs, it can be seen that the proposed MLI is better than the other inverters.



(a) (b)

Fig. 3. Comparison graph of the proposed and other topologies: (a) No. of DC sources vs no. of levels, (b) no. of switching devices vs no. of levels.

V. POWER LOSS CALCULATION

Power losses in any switching device can be divided into three parts:

- Conduction losses (P_C)
- Switching losses (P_{SW})
- Blocking losses (P_B) (normally neglected)

A. Conduction Losses

Conduction losses can be found using drain-source on state resistance (R_{DSON}) and drain current (I_D):

$$P_C = R_{DSON} * {I_D}^2 \quad (1)$$

B. Switching Losses

Switching losses occur due to the fast switching of devices. They include switching on-time (t_{ON}) and off-time (t_{OFF}). Switching losses on t_{ON} can be calculated from (2):

$$P_{SWON} = f_S \int_0^{t_{ON}} V_{ds}(t) i_D(t)\, dt$$

$$P_{SWON} = f_S \int_0^{t_{ON}} \left(\frac{V_{ds}}{t_{ON}} t\right)\left(-\frac{1}{t_{ON}}(t - t_{ON})\right) dt = \frac{1}{6} f_S V_{ds} i_D t_{ON} \quad (2)$$

Similarly, P_{SWOFF} can be found by:

$$P_{SWOFF} = \frac{1}{6} f_S V_{ds} i_D t_{OFF} \quad (3)$$

The total switching losses are given by:

$$P_{SW} = \frac{1}{6} f_S V_{ds} i_D (t_{ON} + t_{OFF}) t_{OFF} \quad (4)$$

where f_s=switching frequency (Hz), V_{ds}= drain to source voltage of the MOSFET, i_D=drain current, t_{ON}= switching on-time, and t_{OFF}=switching off-time.

VI. SIMULATION RESULTS AND DISCUSSION

A. Results

The proposed direct ADC control scheme is simulated in Matlab/Simulink with asymmetric DC sources Vdc, 2Vdc, 4Vdc, and 8Vdc. In simulations and prototype hardware, 12V, 24V, 48V, and 96V isolated DC sources were used. So, the total DC voltage is 180V. Table III shows the simulation parameters in Simulink.

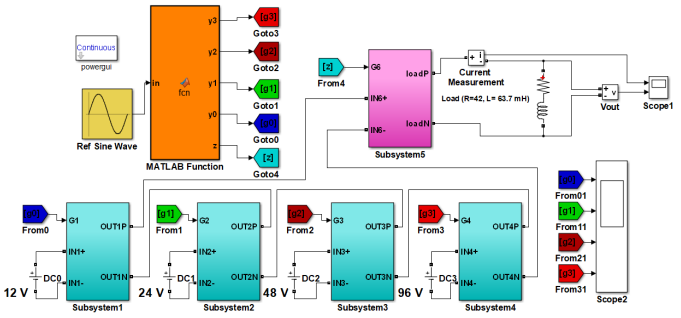


Fig. 4. Matlab/Simulink model.

TABLE III. SIMULATION PARAMETERS

Parameters		Simulation values
Input DC Voltage Sources	DC0	12V
	DC1	24V
	DC2	48V
	DC3	96V
Maximum Output Voltage	Voutmax	180V
Output RMS Voltage	Voutrms	129V
Output current	Ioutrms	2.8A
Output Frequency	*fo*	50Hz
Output Voltage Level at m=1	N_L	31
Power factor	pf	0.90

The 4-bit ADC control scheme is used for the control of the MLI. So, for the 31-level MLI, 4 half-bridge and 1 full-bridge power circuits are used. Figure 4 shows the complete Simulink model. Subsystems 1 to 4 are used for the half-bridge, and subsystem 5 is used for the full-bridge connection. The Matlab function block converts reference AC signal into digital output using 4 bit ADC logic from y0 to y3. z0 gives zero crossings of the reference AC signal. Figure 5 shows the output of the ADC, which works as gate pulses for each half-bridge subsystem, and the zero-crossing signal as a gate pulse for the full-bridge subsystem 5. Each bit has a different frequency, so each half-bridge works at a different switching frequency. Figure 6 shows the output voltage and current waveforms with R=42Ω and L=63.7mH at modulation index m=1. Figure 7 shows the simulated output load voltage and load current waveforms with R=100Ω and L=63.7mH at modulation index m=0.6. The THD of the output voltage varies between 3.16% and 6.42%, with a modulation index from m=1 to 0.5. The THD of the output current is 0.82% at modulation index 1 and 1.69% at 0.5 with a load of L=63.7mH in series with R=42Ω. From Figure 8, it can be seen that the THD of the output current and voltage increase as the modulation index decreases. A passive filter can be used to decrease the THD of the voltage.

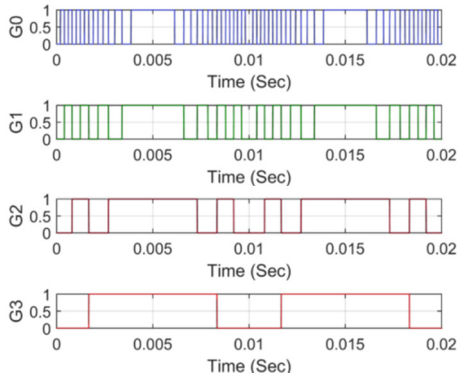


Fig. 5. Output gate pulses from Matlab function block.

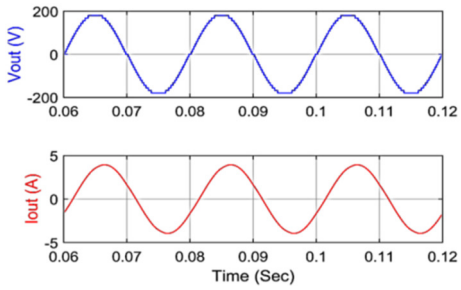


Fig. 6. Output Voltage and current at R=42Ω and L=63.7mH at m=1.0.

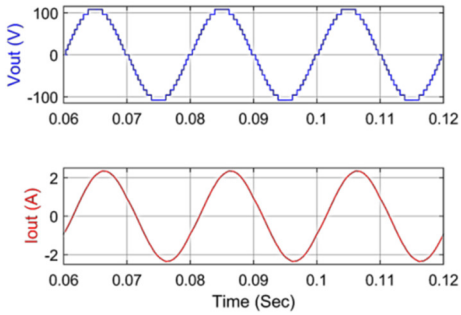


Fig. 7. Output Voltage and current at R=100Ω and L=63.7mH at m=0.6.

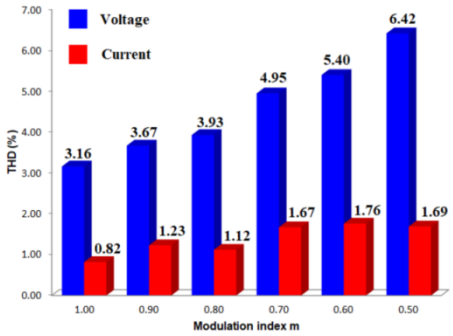


Fig. 8. THD (%) of the output voltage and load current with different values of *m*.

B. Efficiency of the MLI

In the simulations, the total switching losses of the inverter are 19W at load R=42Ω and L=63.7mH. The input power to the inverter is 324W, and the output power is 305W. So, the efficiency of the inverter is 94.13%.

$$\text{Inverter Efficiency} = \text{Output AC power} / \text{Input DC Power} = (V_{orms}*I_{orms}*pf) / (V_{dc}*I_{dc}).$$

VII. HARDWARE RESULTS

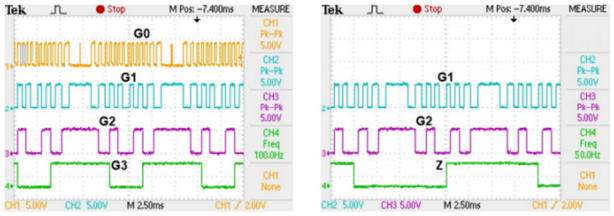
An 8-bit AVR microcontroller was used to generate gate pulses for the prototype hardware model of the proposed MLI. It has six 10-bit on board ADC channels. A reference sine wave was implemented, giving 4-bit digital output and one zero-crossing detector for the implemented power circuit. The generated 4-bit output was used as gate pulses for 4 half-bridges, and the zero-crossing output was used as a gate pulse of a full H-bridge power circuit. An IR 2104 half-bridge driver IC was used for each half-bridge MOSFET. So, a total of 6 IR2104 driver ICs are used for the proposed MLI. IR2104 driver IC has an inbuilt dead-band facility between the upper and lower MOSFETs. No additional hardware or software was required to generate the dead band between the two inverted gate pulses. IRFP460N MOSFETs are used as power switching devices for the full h-bridge circuits, and IRFB4110 MOSFETs are used as power switching devices for the 4 half-bridge circuits. The gate pulses from the microcontroller are isolated using 817 opt-coupler IC to protect the microcontroller. The hardware prototype was tested with a resistive and inductive type of load with different modulation indexes.

The THD of the inverter's output voltage and load current was measured with a Hioki power quality analyzer PQ3198, and the waveforms were captured with a Tektronics Digital Storage oscilloscope. Figure 9(a) shows the output of the ADC of an 8-bit AVR micro-controller that is used as gate pulses (G0, G1, G2, and G3) for the half H-bridges and Figure 9(b) shows the zero crossing output Z as gate pulse of the full H-bridge. Figure 10 shows the output voltage waveform of MLI and its zoomed waveform of a positive half-cycle that clearly shows 31 levels of output.

The TDH of the output voltage was tested with a Hioki make power analyzer which gives 2.11% THD at m=1. The output of the MLI is connected with different load resistances and an inductor of 63.7mH. Figures 11 to 13 show the inverter output voltage and load current waveforms, output current RMS and peak value, total output power, and power factor. Figure 11 shows the output waveforms and the load current THD with power at load resistance of 110Ω in series with an inductor of L=63.7mH. Figure 12 shows the output waveforms and current THD with power at load resistance of 78Ω in series with an inductor of L=63.7mH. Figure 13 shows the output waveforms and current THD with power at load resistance of 60Ω in series with an inductor of L=63.7mH. Figure 14 shows the prototype hardware set-up of complete MLI with load circuits and isolated DC power supplies.

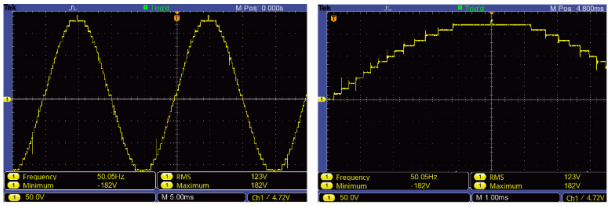
TABLE IV. DEVICE SPECIFICATIONS OF THE HARDWARE PROTOTYPE

Device name	Device number	Specifications
MOSFET	IRFB4110	N-Channel Power MOSFET VDSS = 100V, RDS(on) = 3.7 mΩ, ID = 120 A
MOSFET	IRFP460N	N-Channel Power MOSFET VDSS = 500V, RDS(on) = 0.24 Ω, ID = 20 A
MOSFET Driver	IR2104	Half-bridge Driver IC VOFFSET = 600 V max, Io+/- = 130 mA / 270 mA, VOUT = 10-20 V, ton/off = 680 and 150 ns, Dead time = 520 ns
Photo-coupler IC	PC817	4 pin photo-coupler VCEO = 80 V, Viso(rms) = 5kV
Microcontroller	Atmega328P-PU	8-bit AVR Microcontroller



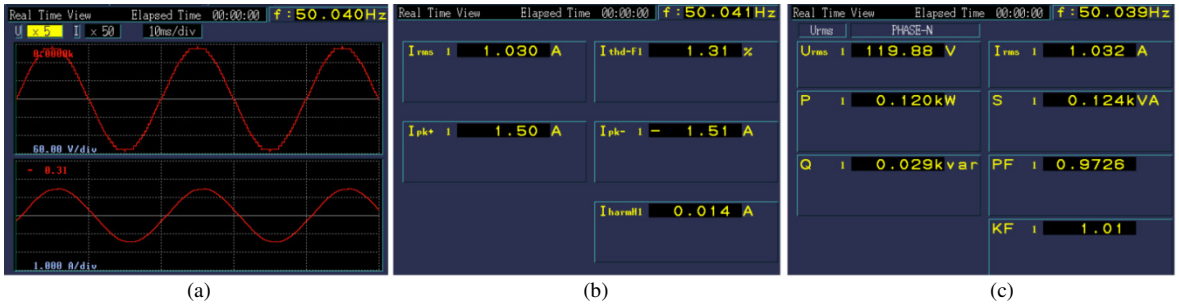
(a) (b)

Fig. 9. Generated gate pulses using ADC: (a) Gate pulses of half-bridges, (b) gate pulse of the full h-bridge.



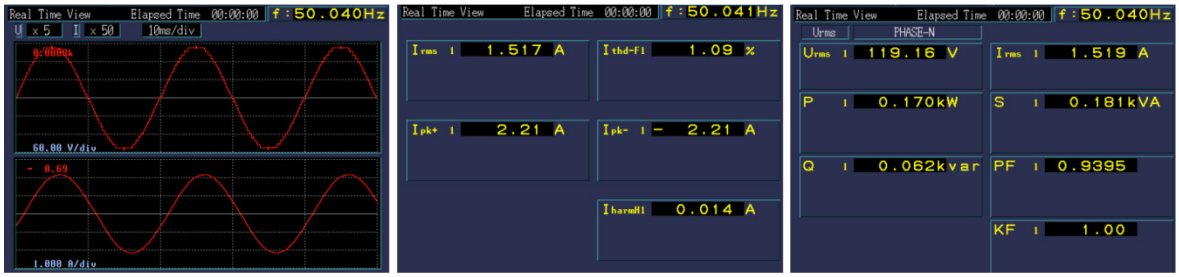
(a) (b)

Hardware prototype results of the ADC-controlled 31-level inverter: (a) Output Voltage, (b) zoomed view.



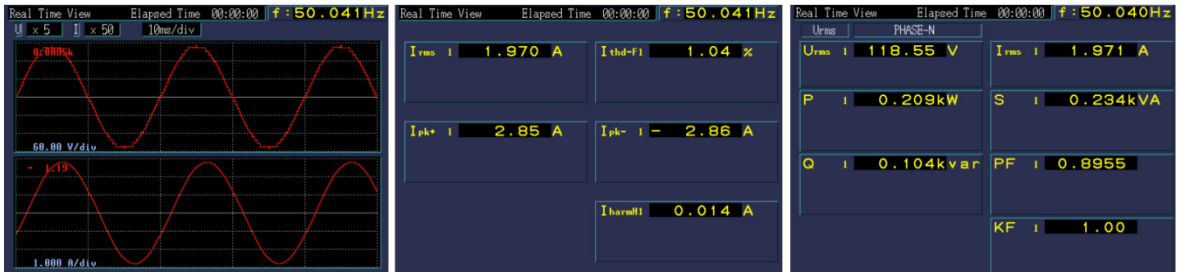
(a) (b) (c)

Fig. 10. Prototype hardware results for R= 110Ω and L=63.7mH at modulation index m=1: (a) Output Voltage and current, (b) RMS value and THD of the output current, (c) pf, active, and reactive power.



(a) (b) (c)

Fig. 11. Prototype hardware results for R= 78Ω and L=63.7mH at modulation index m=1: (a) Output Voltage and current, (b) RMS value and THD of the output current, (c) pf, active, and reactive power.



(a) (b) (c)

Fig. 12. Prototype hardware results for R= 60Ω and L=63.7mH at modulation index m=1: (a) Output Voltage and current, (b) RMS value and THD of the output current, (c) pf, active, and reactive power.

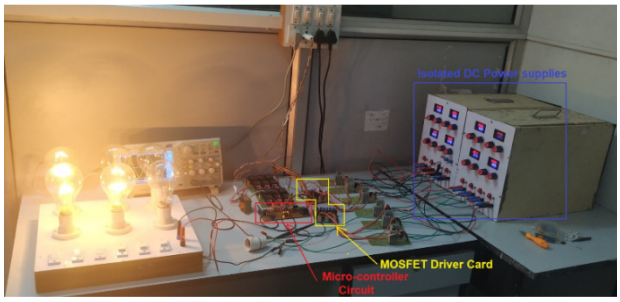


Fig. 13. Prototype hardware set up in the laboratory.

VIII. CONCLUSION

In this paper, binary level DC sources were used to minimize the number of required DC power sources: 31 levels were achieved at the inverter output voltage using direct ADC control and only 4 DC sources. The THD of the inverter output voltage was reduced to 2.11% at m=1 and the THD of the output current was also reduced to 1%. Direct ADC control scheme was used to control power switching devices, which is very simple compared to other control schemes such as SPWM and SVPWM. Here, there is no need to compare the reference sine wave with any carrier (triangular) wave. An inverter's grid connection can be easily implemented using the direct ADC control scheme. The RMS value of the output voltage of the proposed MLI will change according to the changes in the RMS voltage of the grid. Grid frequency and output voltage frequency are always synchronized, which is the main advantage of this control scheme.

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