An Enhanced Z-Source Switched MLI Capacitor for Integrated Micro-Grid with Advanced Switching Pattern Scheme

Budagavi Matam Manjunatha
Department of EEE
Rajeev Gandhi Memorial College of Engineering and Technology
Nandyal, India
manjunath.bmeee@gmail.com

S. Nagaraja Rao
Department of EEE
M. S. Ramaiah University of Applied Sciences
Bengaluru, India
raoeee123@gmail.com

A. Suresh Kumar
Department of EEE
Rajeev Gandhi Memorial College of Engineering and Technology
Nandyal, India
surianisetty@gmail.com

V. Lakshmi Devi
Department of EEE
Sri Venkateswara College of Engineering
Tirupati, India
vldevi.eee@gmail.com

P. Rama Mohan
Department of EEE
Rajeev Gandhi Memorial College of Engineering and Technology
Nandyal, India
rammohan.kadapa@gmail.com

K. Brahmanandam
Department of EEE
Rajeev Gandhi Memorial College of Engineering and Technology
Nandyal, India
brahma181@gmail.com

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Abstract-In this paper, the Enhanced Z-Source Switched Capacitor Multi-Level Inverter (EZSC-MLI) is presented, which can generate a greater number of levels and magnitude in output. The proposed MLI has greater recognition due to its low harmonic profile, fewer switching components, compact size, low switch stress, isolated DC supply, high efficiency, and low cost. A high voltage boost factor is achieved by using the Z-Source. The Switched Capacitor module is used for charging all the capacitors to equal voltage magnitude based on a self-balanced scheme. The proposed topology for grid integration requires dual control loops, a primary voltage control loop, and a secondary current control loop. The performance of the proposed 7-level topology for grid integrated systems is verified with multi-carrier advanced modulation schemes and by simulations carried out in Matlab/Simulink.

Keywords-distributed energy resources; multi-carrier modulation techniques; multi-level inverter; impedance source; renewable energy sources; switched capacitor

I. INTRODUCTION

Nowadays, sustainable and Renewable Energy Sources (RESs) like wind energy and photovoltaic (PV) stacks have been highly recognized as precious substitutions of fossil fuels due to their commercial merits and reliable operation. RESs integrated with power-conditioning systems play a vital role in satisfying the energy demands of a micro-grid system [1]. To improve the energy generation statistics, Distributed Energy Resources (DERs) are introduced. They have less size and easily interfacing methodology. DERs improve the overall system performance by reducing total loss, transformers, and additional devices. Among the DERs, PV stacks are the most promising technology [2]. Generally, a high-voltage gain DC-DC boost converter is required to transform the low-voltage output of the PV to high voltage, which is integrated to the micro-grid by a DC-AC inverter [3]. The maximum duty ratio is restricted due to parasitic resistances and this decreases the overall system stability, causes grounding issues and high dv/dt on switches/diodes.

The above mentioned problems of the two-stage module are discarded by employing an X-shaped impedance circuit, which consists of two inductors and capacitors [4]. With the modish power semi-conductor device, several well-known inverter modules have been amalgamated into grid systems. MLIs are categorized as Diode Clamped (DC-MLI) [5], Flying Capacitor (FC-MLI) [6], and Cascaded H-bridge (CHB-MLI) [7].

The main reasons for producing a number of levels in voltage are: to increase the RMS quality, to decrease the dv/dt stress, and to eliminate large size filters. In MLIs, isolated multiple DC or virtual DC-links are obtained by using transformers or capacitors with the contribution of various switching components. Producing high voltage levels with a low number of isolated DC power supplies and fewer switching devices is the main challenge [8-10]. The suitable approach to limit the DC power supplies is to utilize the capacitors. Yet, additional charge balance strategy is used to intercept the discharging issues [11-13]. Generally, MLI topologies are governed by both fundamental and high switching frequency modulation schemes [14]. The topology with symmetrical and asymmetrical voltage sources is illustrated in [15]. Three phase

Corresponding author: Budagavi Matam Manjunatha

modular topologies are presented in [16-18] with reduced complexity and losses and improved performance. Balanced grid voltage was achieved using the LVRT (Low Voltage Ride Through) control approach in [19]. During a fault state, reactive power is given to ensure protection. The Shunt Var Compensator (SVC) controller was used, it was automatically engaged when a grid fault occurs.

This paper proposes the novel, simple, and efficient EZSC-MLI topology, which is validated by using advanced multi-carrier pulse-width modulation schemes. Dual control loop is used for controlling the voltage and current in the micro-grid system.

II. THE PROPOSED CONCEPT

The configuration of the proposed PV-based EZSC-MLI with grid integrated scheme is depicted in Figure 1. From left to right, the scheme consists of a PV cell, impedance network, Switched Capacitor (SC) module, and a 7-level MLI with dual loop control scheme. The PV supplies energy and feeds the impedance circuit, which transforms the low DC voltage to high DC-link voltage, maintained constant based on the active and shoot through states. The common DC-link voltage is powered by the respective capacitors in the SC module and the entire system is integrated to the micro-grid system through the 7-level inverter. The simplified MLI topology is controlled using advanced modulation schemes. The working and implementation of each unit are described below.

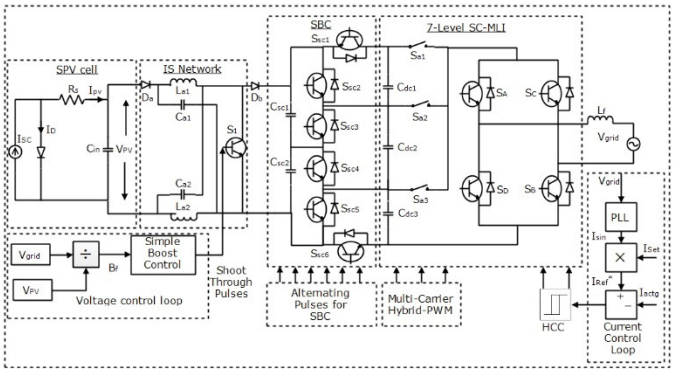

Fig. 1. Configuration of the proposed inverter.

A. PV Source

A PV cell relies on the photo-electric effect to generate electrical energy. A PV cell is similar to a natural diode. When the energy of sunlight is more than the semi-conductor energy gap, current travels via the external circuit system. Based on power level requirements, the PV cell is integrated in parallel and/or in series to attain high current and/or voltage.

$$I_{pv} = I_{sc} - (I_s \left[\exp q \frac{(V_{PV}+R_s Ipv)}{NKT}\right] - 1) - \left[\frac{V_{PV}+R_s Ipv}{R_{sh}}\right] \quad (1)$$

where I_{pv} is the current flowing in PV cell (A), I_{sc} is the reverse saturated diode's current (A), K is Boltzmann's constant, N is Diode's ideality factor, Q is the charge of the electron, T is junction's temperature, R_{sh} and R_s are the shunt and series resistances of the PV cell (Ω), V_{PV} is the PV voltage at the output terminal (V).

B. Z-Source and Self Balancing Module

Generally, VSI accomplishes the buck conversion, which restricts its usage in several areas, such as DER. To amplify the PV input voltage, a two-stage boost conversion methodology is used, which requires additional switching devices, stage and control scheme. Using an impedance network in X-shape will reduce the complexity. High voltage gain is achieved at output terminals by furnishing shoot through state. This state is possible when the lower and upper switches in the same leg are conducted simultaneously and it is not possible while using a multi-level inverter. The Z network with single switch is proposed, since it reduces the complexity of control. The voltage across the traditional ZSI is:

$$V_{ZSI,trad} = 2 \times V_L - V_{pv} \quad (2)$$

Boost factor (B_f) and the peak AC voltage (V_o) are given by:

$$B_{f,trad} = \frac{1}{1-\frac{2\times T_{sh}}{T}} \quad (3)$$

$$V_{o,trad} = B_{f,trad} \times V_{pv} \quad (4)$$

where V_L and V_{pv} are the voltage across the Z source inductor and the input. Various methods are used to overcome the unbalanced voltage problems such as, feedback methods [20] or the regulated switching pattern scheme [21]. The SC balanced technique is very popular because it does not require a feedback method or continuous monitoring. The proposed switched capacitor module consists of two input capacitors C_{s1}, C_{s2}, three output capacitors C_1, C_2, C_3, and six switches S_{c1} to S_{c6}. The modes of operation are depicted in Figure 2.

In Mode-I (Figure 2(a)), all odd numbered switches will conduct. The capacitors C_{s1}, C_{s2} charge the C_1 and C_2 capacitors, thus the voltage across the C_1 (V_{cs1}) is V_{c1} and the voltage of capacitor C_2 is V_{cs2}. In Mode-II (Figure 2(b)), all even numbered switches will conduct. The capacitors C_{s1}, C_{s2} charge the C_2 and C_3 capacitors, thus V_{cs1}=V_{c2} and V_{cs2}=V_{c3}. The voltages across C_{s1}, C_{s2}, C_1, C_2, and C_3 are:

$$V_{cs1} = V_{cs2} = \left(\frac{V_{pv}}{2}\right) \quad (5)$$

$$V_{c1} = V_{c2} = V_{c3} = \left(\frac{V_{in}}{2}\right) \quad (6)$$

where V_{dc} is the output voltage of the Z network. The maximum available output voltage across the inverter $V_{o,inv}$ is:

$$V_{o,inv} = V_{c1} + V_{c2} + V_{c3} \quad (7)$$

$$V_{o,inv} = \left(\frac{V_{dc}}{2}\right) + \left(\frac{V_{dc}}{2}\right) + \left(\frac{V_{dc}}{2}\right) \quad (8)$$

$$V_{o,inv} = \left(\frac{3}{2}\right).V_{dc} \quad (9)$$

From (8) and (9), it is clear that voltage is balanced and boosted by 1.5 times. The capacitors C_{s1}, C_{s2} are powered by the ZSI module. The output of the Z network is given by the SC module. By considering the boost factor of 1.5, (4) and (5) can be rewritten to get the boost factor and the peak output of the enhanced Z network with the self-voltage balancing network.

$$B_{f,Enh} = \frac{1.5}{1-\frac{2\times T_{sh}}{T}} \quad (10)$$

$$V_{o,Enh} = B_{f,Enh} \times (V_{in}) \quad (11)$$

where T_{sh}/T represents the duty ratio of shoot through state, the peak output voltage of EZSC-MLI is 1.5 times greater than TZSI with and/or without shoot through state.

The graphical representation of Boost factor vs T_{sh}/T and peak voltage vs T_{sh}/T for TZSI and EZSI topologies are depicted in Figures 3 and 4. If the shoot through ratio lies in between 0 to 0.4, the design procedure for passive devices is the same for the two ZSI modules. For any given T_{sh}/T, the peak output voltage and the boost factor of EZSC-MLI are constantly 1.5 times higher than TZSI's, hence this network is named as an enhanced network [14]. If T_{sh}/T is 0.4, the boost factor of TZSI is 5 and EZSC-MLI is 7.5 and the corresponding peak output voltages are 500V and 750V (for input voltage of 100V). The proposed 7-level EZSC-MLI is integrated to a micro-grid.

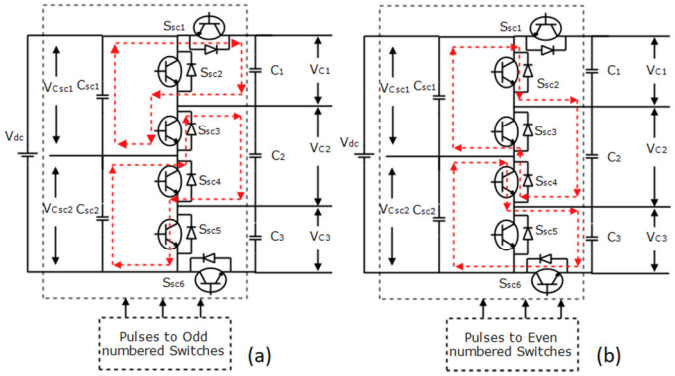

Fig. 2. Operating modes of the SC circuit: (a) Odd number switching, (b) even number switching.

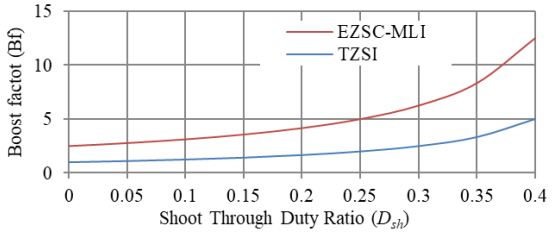

Fig. 3. Boost factor vs T_{sh}/T.

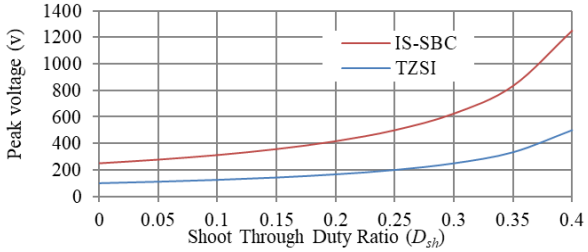

Fig. 4. Peak voltage vs T_{sh}/T.

C. ControlLloops

In the proposed concept, dual control loops are utilized, i.e. the primary voltage control loop and the secondary current control loop. The aim of the primary loop is to regulate the output voltage of the Z-source network, by changing the shoot through duty ratio as specified in (10). This maintains the MLI voltage constant and greater than the grid voltage. A reference voltage signal is obtained by comparing the PV voltage and the grid voltage. The outcome is compared with the triangular carrier signal to produce the shoot through state duty ratio. The aim of the current loop is the injection of the reference current to the grid within the harmonic standards of IEEE-519. Grid synchronization requires the inverter output voltage, frequency and phase should match with the grid. This is furnished by single-phase Phase-Locked Loop (PLL) circuitry.

The PLL circuit generates the required phase sequence and fundamental frequency as a current shape (I_{sin}) which is multiplied with the reference magnitude of current (I_{ref}) established as final reference current (I_{ref}*). I_{ref}* is compared with the actual grid current (I_{act}) and the outcome is imparted to the Hysteresis Current Controller (HCC) for the generation of the switching states to the H-bridge module [22] in the 7-level MLI. The ON/OFF states of the respective switches in the H-bridge module are highly demanded based on the reference grid current.

III. MODULATION SCHEME

The working principles of the 7-level MLI are level generation and polarity generation. The level generation module has three switches S_1, S_2, and S_3, which convert the constant DC-link voltage to DC levels. The switching sequence for DC-level generation of the 7-level MLI is depicted in Table. I. On the other side, polarity generation has four switches, S_A, S_B, S_C, and S_D, which convert the DC-level voltage to AC voltage and are controlled by the secondary current control loop. The switching sequence for polarity generation is depicted in Table II, where *N* represents the ON-state of the switch and *F* represents the OFF-state of the switch.

TABLE I. SWITCHING STATES OF DC-LEVEL GENERATION

Vo	***S1***	***S2***	***S3***
V_{dc}	*N*	*F*	*F*
$2V_{dc}/3$	*F*	*N*	*F*
$V_{dc}/3$	*F*	*F*	*N*

TABLE II. SWITCHING STATES OF POLARITY GENERATION

Vo	**S_A**	**S_B**	**S_C**	**S_D**
0	*F/N*	*N/F*	*F/N*	*N/F*
Positive	*N*	*N*	*F*	*F*
Negative	*F*	*F*	*N*	*N*

The switches in the level generation scheme are controlled by advanced modulation schemes, such as the level-shifted multi-carrier modulation (LSPWM) scheme, the phase-angled (PAPWM) scheme, and the variable switching frequency (VSFPWM) scheme.

A. The Multi-Carrier Level-Shifted PWM (LSPWM) Scheme

In the well-known control action of LSPWM, all respective carriers are shifted by time. For *n* voltage levels, *n*-1 carriers are pre-requisite adjoining each other for the production of the switching pattern. The peak amplitude of triangular carrier wave-shape is differed and it is equivalent to the reference

sinusoidal voltage as a summation of all carrier-waves. High switching frequency is used. Generally it depends on multiplication factor and fundamental frequency. The frequency value of the carrier is measured by:

$$F_c = M_f \times F_f \quad (12)$$

where F_c denotes carrier frequency (Hz), M_f denotes the multiplication factor, with an odd value more than 11, and F_f denotes the fundamental frequency value (Hz). The modulation index of the pulse-width modulation scheme is:

$$MI_a = \frac{V_r}{V_{c\,(m-1)}} \quad (13)$$

where V_r. V_c denote the peak amplitudes of reference and carrier triangular wave-shapes. The production of switching states is done by relating the reference and carrier wave-shapes. When the reference wave is greater than the carrier wave, a particular switch is in the ON state and/or when it is less than the carrier wave, a particular switch is in the OFF state. The LSPWM schemes are: Phase Disposed (PD), Phase Opposed Disposed (POD), Alternate Phase Opposed Disposed (APOD). The PD based carrier waveform is depicted in Figure 5.

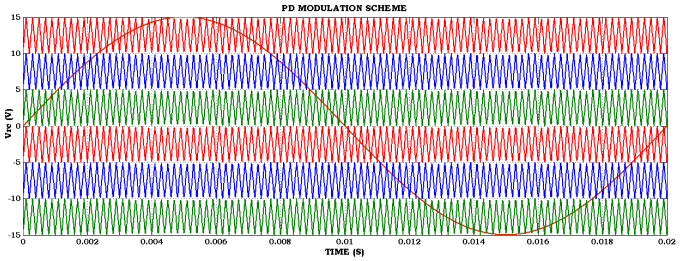

Fig. 5. PD modulation scheme.

B. Multi-Carrier Phase-Angle Shifted PWM (PAPWM)

The PAPWM scheme shown in Figure 6 is the same with level-shifted modulation. All the carriers have equal switching frequencies and different peak amplitudes, which are vertically disposed by a certain phase-angle to vanquish the phase imbalance issues and unbalanced voltages [22]. The disposed phase-angle ($\emptyset_{ps}$) is given by,

$$\emptyset_{ps} = \frac{360^{\circ}}{M_f\,(m-1)} \quad (14)$$

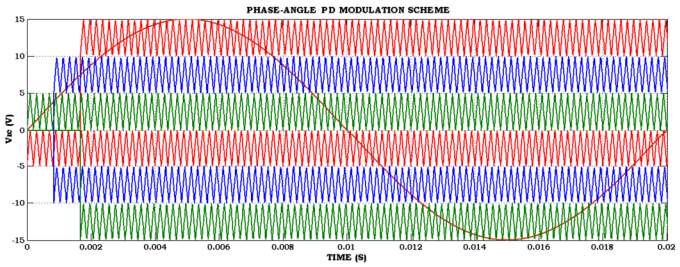

Fig. 6. PAPWM scheme.

C. Multi-Carrier Variable Switching Frequency (VSFPWM)

The VSFPWM scheme is the same with the level-shifted modulation scheme. All the carriers have different peak amplitudes and unequal switching frequencies such as 5050Hz, 7050Hz, and 9050Hz. These frequencies are selected with respect to the multiplication factor. This modulation technique has better minimization of harmonic distortions and low switch stress and increased efficiency, while it requires low-rated filter units. The VSFPWM scheme is depicted in Figure 7.

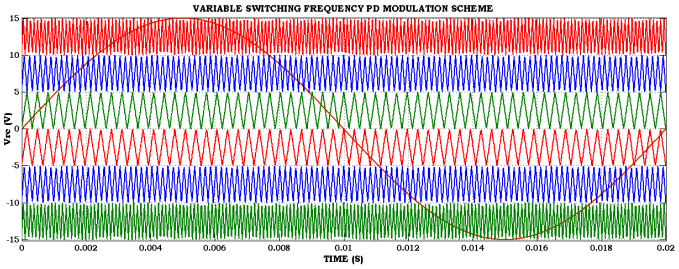

Fig. 7. VSFPWM scheme.

D. Modified Modulation Scheme

A unique modulation scheme is introduced by utilizing PA and VSFPWM schemes for getting optimal switching states. All the carriers in the proposed modulation scheme have different peak amplitudes which are vertically disposed by the respective phase-angles and have unequal switching frequencies such as 5050Hz, 7050Hz, and 9050Hz with respect to the multiplication factor. The advanced modulation scheme is depicted in Figure 8.

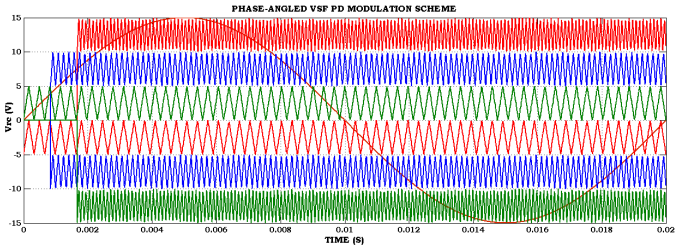

Fig. 8. Advanced PD modulation scheme.

IV. SIMULATION RESULTS

The performance of the ZSI based 7-level SC-MLI fed grid-integrated system with several modulation schemes is validated in Matlab/Simulink and is developed with the help of the operating parameters shown in Table III. Figure 9(a) shows the complete Matlab model, Figure 9(b) shows the hysteresis controller, and Figure 9(c) shows the controller for generating shoot through pulses.

TABLE III. OPERATING PARAMETERS

Parameter	Value
PV Source	V_{pv}=100V
Grid Voltage & frequency	V_g=230V, F_g=50Hz
Impedance source	L_1=L_2= 10mH. C_1=C_2= 0.01F
DC-link voltage	150V
Switching frequency	10KHz
DC-link capacitor	C_{dc}= 0.01F
Capacitors	C_1=C_2= C_3 = 0.01F

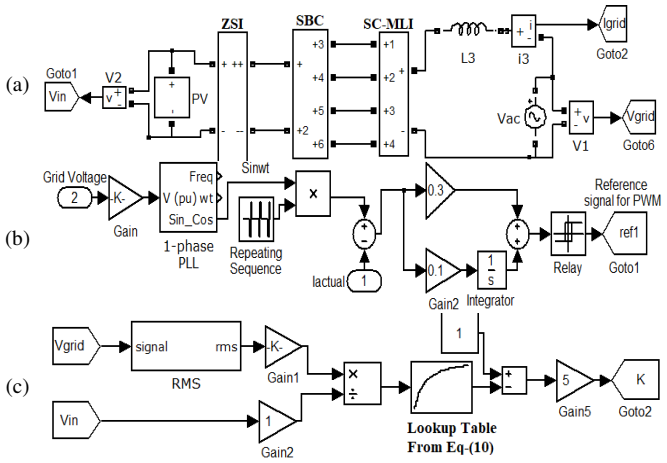

Fig. 9. Matlab/Simulink model.

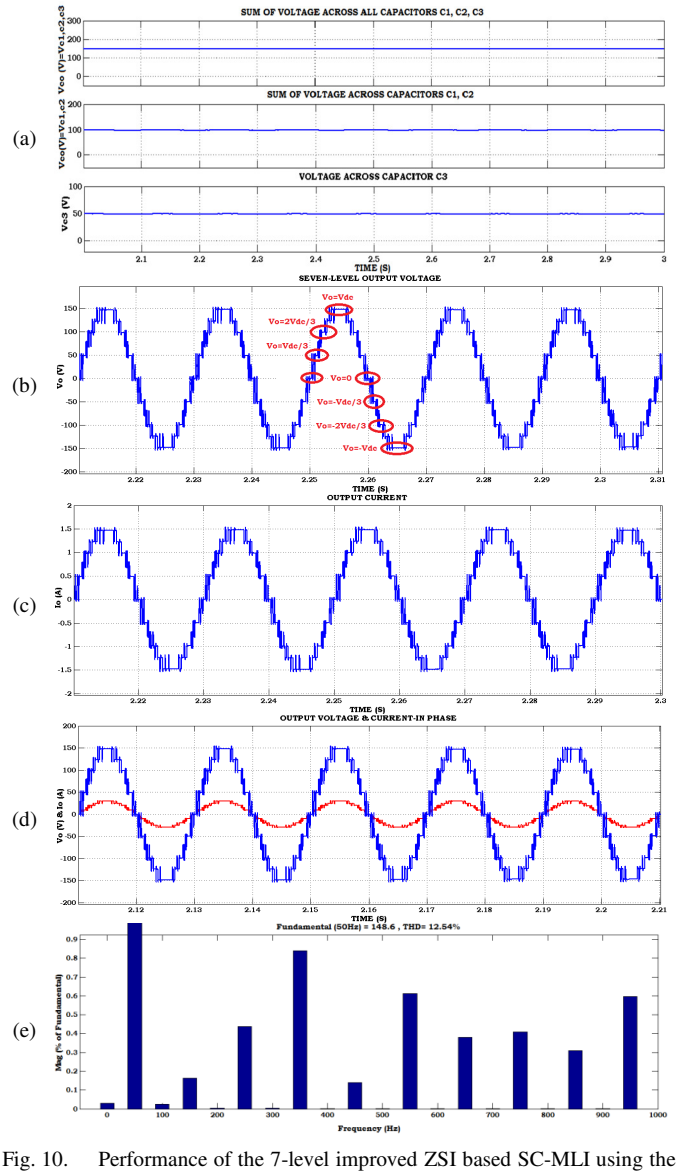

Fig. 10. Performance of the 7-level improved ZSI based SC-MLI using the proposed advanced modulation technique. (a) Voltage across the capacitors, (b) 7-level output Voltage, (c) output current, (d) output Voltage and current-in phase, and (e) THD of the output Voltage.

A. Performance Evaluation of the Proposed Topology with Advanced Modulation Techniques in a Standalone System

Figure10 shows the simulation outcome of the 7-level ZSI based SC-MLI with advanced modulation scheme. From Figure 10(e), it is observed that the harmonic content in the output voltage is high at odd multiples of the fundamental frequency. The PV input voltage 100V is transformed into 150V DC-link voltage by the SC module. The DC-link capacitor voltages are maintained constant and balanced for achieving the significant 7-level output. The THD of the output voltage is 12.54%. The performance of the proposed 7-level SC-MLI is evaluated by classical and the proposed PWM schemes. It can be seen that the proposed advanced modulation scheme has better features. The THD analysis of the modulation schemes is depicted in Figure 11.

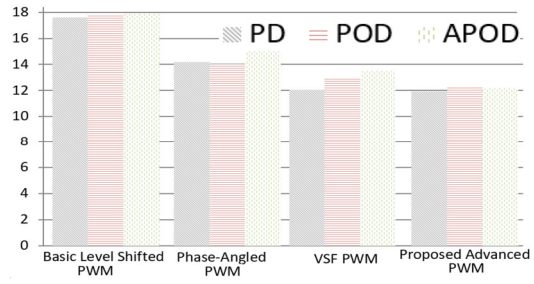

Fig. 11. THD analysis of the considered modulation schemes.

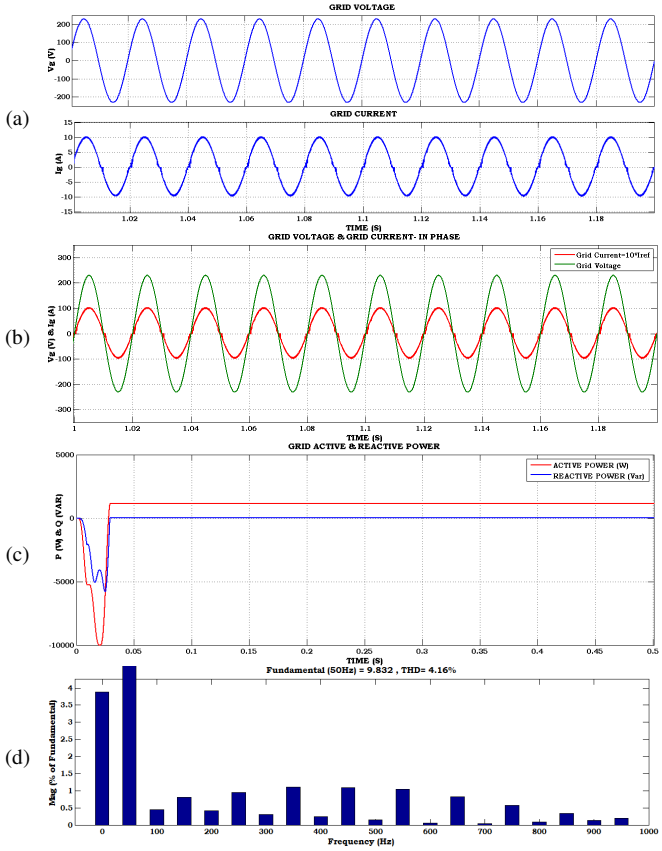

Fig. 12. Performance of the 7-Level ZSI integrated to the grid. (a) Grid Voltage and current, (b) in-phase grid voltage and current component, (c) grid active and reactive power, (d) THD of grid current.

B. Grid Integration Scheme

The proposed topology is integrated to a micro-grid with the advanced modulation technique. Figure 12 represents the simulation outcome of the 7-level EZSC-MLI with the advanced modulation scheme integrated to the grid with low-rated filter units. The attained grid voltage and current are pure-sinusoidal and maintained constant at the fundamental frequency. Both the components are in-phase representing a unity power factor. The THD of the grid current is 4.16%, well within IEEE-519 standards.

V. CONCLUSIONS

In this paper, the enhanced Z-source SC-MLI topology with various modulation techniques is proposed. It is capable of operating with a high voltage gain factor. The proposed SC-MLI utilizes only a single PV source and 7 active switches for the production of 7 voltage levels. Effective modulation schemes are used for the generation of optimal switching states. They have better reduction of harmonic distortion over the classical schemes and attain favorable benefits. There is no need of additional balancing technique, a self-balancing technique is initiated which reduces the complex control circuitry. When using the proposed 7-level SC-MLI topology, the switching components are fewer over the classical MLI topologies. The proposed inverter topologies are more suitable for the DER fed grid by utilizing attractive voltage and current control loops. This system can be used for integrating different renewable energy sources.

REFERENCES

[1] M. A. Hannan, S. Y. Tan, A. Q. Al-Shetwi, K. P. Jern, and R. A. Begum, "Optimized controller for renewable energy sources integration into microgrid: Functions, constraints and suggestions," *Journal of Cleaner Production*, vol. 256, May 2020, Art. no. 120419, https://doi.org/10.1016/j.jclepro.2020.120419.

[2] L. M. Castro, J. R. Rodríguez-Rodríguez, and C. Martin-del-Campo, "Modelling of PV systems as distributed energy resources for steady-state power flow studies," *International Journal of Electrical Power & Energy Systems*, vol. 115, Feb. 2020, Art. no. 105505, https://doi.org/10.1016/j.ijepes.2019.105505.

[3] M. Kwon and S. Choi, "Control Scheme for Autonomous and Smooth Mode Switching of Bidirectional DC–DC Converters in a DC Microgrid," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 7094–7104, Dec. 2018, https://doi.org/10.1109/TPEL.2017.2753845.

[4] F. Z. Peng, M. Shen, and Z. Qian, "Maximum boost control of the Z-source inverter," *IEEE Transactions on Power Electronics*, vol. 20, no. 4, pp. 833–838, Jul. 2005, https://doi.org/10.1109/TPEL.2005.850927.

[5] J. Wang, J. Wang, B. Xiao, Z. Gui, and W. Jiang, "Full Range Capacitor Voltage Balance PWM Strategy for Diode-Clamped Multilevel Inverter," *Electronics*, vol. 9, no. 8, Aug. 2020, Art. no. 1263, https://doi.org/10.3390/electronics9081263.

[6] A. Rahmati, M. Arasteh, S. Farhangi, and A. Abrishamifar, "Flying Capacitor DTC Drive with Reductions in Common Mode Voltage and Stator Overvoltage," *Journal of Power Electronics*, vol. 11, no. 4, pp. 512–519, 2011, https://doi.org/10.6113/JPE.2011.11.4.512.

[7] S. Ray, N. Gupta, and R. A. Gupta, "A Comprehensive Review on Cascaded H-bridge Inverter-Based Large-Scale Grid-Connected Photovoltaic," *IETE Technical Review*, vol. 34, no. 5, pp. 463–477, Sep. 2017, https://doi.org/10.1080/02564602.2016.1202792.

[8] P. R. Bana, K. P. Panda, and G. Panda, "Performance evaluation of a reduced components count single-phase asymmetric multilevel inverter with low standing voltage," *International Transactions on Electrical Energy Systems*, vol. 30, no. 8, 2020, Art. no. e12430, https://doi.org/10.1002/2050-7038.12430.

[9] N. Vishwajith, S. N. Rao, and S. Sachin, "Performance analysis of reduced switch ladder type multilevel inverter using various modulation control strategies," *Journal of Physics: Conference Series*, vol. 1706, no. 1, Sep. 2020, Art. no. 012092, https://doi.org/10.1088/1742-6596/1706/1/012092.

[10] B. M. Manjunath, D. V. Ashok Kumar, and M. Vijaya Kumar, "A Simplified PWM Technique for Isolated DC-DC Converter Fed Switched Capacitor Multi-Level Inverter for Distributed Generation," *International Journal of Power Electronics and Drive Systems*, vol. 8, no. 3, pp. 1230–1239, Sep. 2017, https://doi.org/10.11591/ijpeds.v8.i3.pp1230-1239.

[11] S. N. Rao, D. V. Ashok Kumar, and Babu, "Integration of Reversing Voltage Multilevel Inverter Topology with High Voltage Gain boost Converter for Distributed Generation," *International Journal of Power Electronics and Drive Systems*, vol. 9, no. 1, pp. 210–219, Mar. 2018, https://doi.org/10.11591/ijpeds.v9.i1.pp210-219.

[12] M. Budagavi Matam, A. K. Devarasetty Venkata, and V. K. Mallapu, "Evaluation of Impedance network Based 7-Level Switched Capacitor Multi Level Inverter for Single Phase Grid Integrated System," *Journal of The Institution of Engineers (India): Series B*, vol. 99, no. 6, pp. 623–633, Dec. 2018, https://doi.org/10.1007/s40031-018-0348-2.

[13] P. Omer, J. Kumar, and B. S. Surjan, "A Review on Reduced Switch Count Multilevel Inverter Topologies," *IEEE Access*, vol. 8, pp. 22281–22302, 2020, https://doi.org/10.1109/ACCESS.2020.2969551.

[14] Z. Boussada, O. Elbeji, and M. Benhamed, "Different topologies and control techniques of multi level inverter: A literature survey," in *2017 International Conference on Green Energy Conversion Systems (GECS)*, Hammamet, Tunisia, Mar. 2017, https://doi.org/10.1109/GECS.2017.8066187.

[15] B. M. Manjunatha, S. N. Rao, A. S. Kumar, K. S. Zabeen, S. Lakshminarayanan, and A. V. Reddy, "An Optimized Multilevel Inverter Topology with Symmetrical and Asymmetrical DC Sources for Sustainable Energy Applications," *Engineering, Technology & Applied Science Research*, vol. 10, no. 3, pp. 5719–5723, Jun. 2020, https://doi.org/10.48084/etasr.3509.

[16] A. Nouaiti, A. Saad, A. Mesbahi, M. Khafallah, and M. Reddak, "Design and Test of a New Three-Phase Multilevel Inverter for PV System Applications," *Engineering, Technology & Applied Science Research*, vol. 9, no. 1, pp. 3846–3851, Feb. 2019, https://doi.org/10.48084/etasr.2573.

[17] D. A. Tuan, P. Vu, and N. V. Lien, "Design and Control of a Three-Phase T-Type Inverter using Reverse-Blocking IGBTs," *Engineering, Technology & Applied Science Research*, vol. 11, no. 1, pp. 6614–6619, Feb. 2021, https://doi.org/10.48084/etasr.3954.

[18] T. Demirdelen, R. I. Kayaalp, and M. Tumay, "A Modular Cascaded Multilevel Inverter Based Shunt Hybrid Active Power Filter for Selective Harmonic and Reactive Power Compensation Under Distorted/Unbalanced Grid Voltage Conditions," *Engineering, Technology & Applied Science Research*, vol. 6, no. 5, pp. 1133–1138, Oct. 2016, https://doi.org/10.48084/etasr.777.

[19] S. A. Dayo, S. H. Memon, M. A. Uqaili, and Z. A. Memon, "LVRT Enhancement of a Grid-tied PMSG-based Wind Farm using Static VAR Compensator," *Engineering, Technology & Applied Science Research*, vol. 11, no. 3, pp. 7146–7151, Jun. 2021, https://doi.org/10.48084/etasr.4147.

[20] Z. Ramli, J. Jamaludin, N. Abd Rahim, and S. R. Azzuhri, "Capacitor Voltage Balancing with Online Controller Performance-Based Tuning for a Switch-Sharing-Based Multilevel Inverter," *Applied Sciences*, vol. 11, no. 10, Jan. 2021, Art. no. 4428, https://doi.org/10.3390/app11104428.

[21] A. Moghassemi and S. Padmanaban, "Dynamic Voltage Restorer (DVR): A Comprehensive Review of Topologies, Power Converters, Control Methods, and Modified Configurations," *Energies*, vol. 13, no. 16, Jan. 2020, Art. no. 4152, https://doi.org/10.3390/en13164152.

[22] T. Nguyen-Van, R. Abe, and K. Tanaka, "A Digital Hysteresis Current Control for Half-Bridge Inverters with Constrained Switching Frequency," *Energies*, vol. 10, no. 10, Oct. 2017, Art. no. 1610, https://doi.org/10.3390/en10101610.