A Review on Energy Efficient CMOS Digital Logic

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Abstract— Autonomy of power supply used in portable devices directly depends on energy efficiency of digital logic. This means that digital systems, beside high processing power and very complex functionality, must also have very low power consumption. Power consumption depends on many factors: system architecture, technology, basic cells topology-speed, and accuracy of assigned tasks. In this paper, a review and comparison of CMOS topologies techniques and operating modes is given, as CMOS technology is expected to be the optimum choice in the near future. It is shown that there is a full analogy in the behavior of digital circuits in sub-threshold and strong inversion. Therefore, synthesis of digital circuits is the same for both strong and weak operating modes. Analysis of the influence in inversion. Therefore, synthesis of digital circuits is the same for both strong and weak operating modes. Analysis of the influence in the operating area in the sub-threshold regime is overlapped with the area of a disconnected transistors in strong inversion regime, current ratio in on and off the state has been significantly reduced. Consequently, CMOS circuit logic delay

I. INTRODUCTION

Designers of digital circuits are confronted with two often conflicting demands: how to achieve higher operating speeds and lower energy consumption. Usually, the same circuit family could not satisfy both demands at the same time, i.e. high-speed circuits have high level of consumption and vice versa. That’s how series of integrated circuits called low-power circuits or high-speed circuits were created. Optimally designed digital system includes a variety of different series of the same integrated circuits’ family.

Today, as the whole digital system is manufactured as a single integrated circuit, the designing problem is reduced to the choice of a design that can ensure maximum energy efficiency. That implies the design with minimum power consumption inside the specified frequency range or maximum operating speed for a given energy consumption level. The usage of low-power sources of power supply, which collect their primary energy from the environment, has increased lately. Thus, the art of design of low power circuits is brought down to the selection of optimal (intelligent) solutions that will reduce the speed of information processing as much as possible, without violating certain system characteristics. Such an optimal project implies the decomposition of the system architecture, good choice of the circuit topology that will provide the optimal synthesis of different functions in the defined architecture, and good choice of the circuit design technology. This requires the designer to be familiar with components, circuits and systems. Consumption of each system is determined using the following five guidelines of each project: given task, technology, circuit topology, operating speed and accuracy. Since these five guidelines can be placed on the fingers of one hand, they are known as “low-power hand” [1]. Therefore, optimization of energy consumption is a multidimensional problem that requires taking into consideration the level of consumption at each stage of the VLSI integrated circuit design. The biggest savings of electrical energy consumption (10 to 20 times), with least waste of time (at the level of a minute) is done in the early stages of designing, in which the project is presented as a set of abstract communication tasks [2]. The application of optimization techniques and consumption provides an estimation at each project stage, leading to optimal consumption project [3]. At lower levels of the design (transistor, deployment and connectivity), possible energy savings are significantly lower (10 to 20%), and time estimation can last for days, because the project is presented with all detail. Thus, it is necessary to process a very large amount of data [3]. CMOS digital circuits’ technology based on silicon will most likely be dominant for the next twenty years or more [4, 5, 6], with standard low power consumption, technology for reducing the transistor size to a scale of about ten nanometers and operating speed in the GHz domain. During the last ten years, more attention from researchers as well as manufacturer of integrated circuits is paid to digital CMOS circuits operating in the sub-threshold (weak inversion) regime. Supply voltage in this regime is lower than the threshold voltage $V_t$ of MOS transistors $(V_{dd}<V_t)$ and is about a few hundred millivolts. Thanks to that fact, the dynamic consumption level is significantly reduced in regard to CMOS circuits operating in the strong inversion regime. Since the operating area in the sub-threshold regime is overlapped with the area of a disconnected transistors in strong inversion regime, current ratio in on and off the state has been significantly reduced. Consequently, CMOS circuit logic delay
in the sub-threshold regime is several orders of magnitude higher.

Designers of CMOS digital devices, especially portable ones, have a challenging requirement: how to ensure high processing power and very complex functionality along with low power consumption. Certainly part of the solution is a proper choice of CMOS technology as well as weak and strong inversion regime operating areas.

Although MOS transistor static characteristics in weak inversion and strong inversion regimes are functionally very different, it will be shown that there is an absolute analogy in the behavior and functional dependency of CMOS circuit parameters in those regimes. Thanks to that, design techniques of more complex CMOS circuits are the same in sub-threshold and strong inversion regime. This fact considerably facilitates designer’s work of MOS circuit in a sub-threshold regime and enables faster development.

Optimal consumption generally does not mean minimal consumption. Minimal consumption and minimal logic delay are mutually opposite requirements. Taking into account only the minimization of consumption, a project with unacceptable logic delay could be delivered. The consumption as well as the logic delay of CMOS circuit depends on MOS transistor threshold voltage \( V_t \) and supply voltage \( V_{dd} \). Because of that, one part of this paper is devoted to consumption optimization techniques in systems with multiple levels of \( V_t \) and \( V_{dd} \).

Specific part of this paper refers to the big toe of “low-power hand”-- topologies. Review of topologies of CMOS logic series that ensure low-power within the specified range of operating frequencies is given, which implies their use in both strong and weak inversion regimes.

The analysis is based on simplified current-voltage models of MOS transistors and PSPICE software using parameters of 180 nm technology.

II. CMOS OPERATING IN THE WEAK INVERSION REGIME

In essence, there are three areas of MOS transistor static characteristics [7]. Figure 1 shows the logarithmic dependence of nMOS transistor drain current as a function of gate-source voltage \( (V_{ds}) \), at a constant drain-source voltage \( (V_{ds}) \) and source-substrate voltage \( (V_{ss}) \). In the literature, the smallest attention is paid to the medium (moderate) area which is mostly considered as a part of strong inversion threshold area [8, 9]. In digital circuits, it is assumed that \( V_{gs} > V_t \), where \( V_t \) is a MOS transistor’s threshold voltage, transistor is operating in strong inversion regime, and for \( V_{gs} < V_t \) in the sub-threshold (weak inversion) regime. Therefore, from today’s application point of view, it can be said that \( V_t \) is a gate-source voltage on a border between the weak and the strong inversion regime.

It is a well-known fact that the \( I_d(V_{ds}, V_{gs}) \) characteristic in the strong inversion regime has two areas: non-saturated and saturated. In the non-saturated area, it holds that \( I_d \propto V_{gs} \) and \( I_d \propto V_{ds} \), while in saturated area \( I_d \propto V_{gs}^2 \) and \( I_d \propto f(V_{ds}) \), that is \( I_d \approx \text{const} \) as a function of \( V_{ds} \).

MOS transistor characteristics in the weak inversion regime are defined as follows:

\[
I_{\text{weak inv}} = \begin{cases} 
I_0 e^{\frac{V_{gs} - V_t}{nV_t}} & (1 - e^{-V_{gs}/nV_t}), V_{ds} < 3\phi_t, \text{ non-saturated area} \\
I_0 e^{\frac{V_{gs} - V_t}{nV_t}} & , V_{ds} > 3\phi_t, \text{ saturated area}, 
\end{cases}
\]

where

\[
I_0 = \mu C_{\text{ox}} \frac{W}{L} (n-1) \phi_t^2
\]

is a drain current on a border between weak and strong inversion.

![Fig. 1. log I_d characteristic as a function of V_g, at a constant V_d and V_t.](image)

The meaning of the parameters in (1) and (2) are the following: \( \mu \) is a mobility of major charge carriers (electrons and holes in nMOS to pMOS transistor), \( C_{\text{ox}} = \varepsilon_{\text{ox}} / t_{\text{ox}} \) is gate capacitance \( (\varepsilon_{\text{ox}} \) is a dielectric constant, \( t_{\text{ox}} \) is a thickness of the gate oxide), \( W \) and \( L \) are the width and length of the channel, respectively, \( \phi_t = kT/q \) is a thermal potential \( (q = 26 \text{ mV at } T=300K) \), where \( n = 1 + C_d/C_{\text{ox}} = 1.5 \) is a gradient factor.

For \( V_{ds} > 3\phi_t \), drain current is almost independent of the voltage \( V_{ds} \) (Figure 2), so that the area analogous to strong inversion regime, can be treated as saturated area. In this area it holds \( I_d \approx e^{V_{gs}^2} \) . For \( V_{ds} < 3\phi_t \), at \( V_{gs} = \text{const.} \), \( I_d \approx e^{V_{gs}} \), transistor is in the non-saturated area.

Thanks to the analogy in the field of MOS transistor characteristics, there is an appropriate analogy of operation and CMOS logic circuit characteristics [8]. Thus, for example, voltage and current static characteristics in the weak inversion regime (Figure 3) have the same shape as in the strong inversion regime. Even inverter threshold voltage \( V_{\text{th}} \) is
obtained in the same way – equating of nMOS and pMOS drain currents in the saturated area of characteristics.

\[ V_{T_{\text{sub}}} = \frac{V_{dd_{\text{sub}}}}{2} - \frac{n \phi_i}{2} \ln \left( \frac{I_{on}}{I_{op}} \right) \]  \hspace{1cm} (3)

and maximal current from the voltage source:

\[ I_{dd_{\text{sub}}} = I_{on} \frac{V_{dd_{\text{sub}}}/2-V_t}{V_{dd_{\text{sub}}}-V_t} \]  \hspace{1cm} (4)

where

\[ 3\phi_i < V_{dd_{\text{sub}}} < V_i = V_{in} = V_{op} \]  \hspace{1cm} (5)

is a supply voltage, \( V_{in} \) and \( V_{op} \) threshold voltages, and \( I_{on} \) and \( I_{op} \) currents on the border between weak and strong inversion of nMOS and pMOS transistors, respectively. For a symmetric inverter (\( I_{on}=I_{op} \)), threshold voltage is, just like in strong inversion regime, \( V_{T_{\text{sub}}} = V_{dd_{\text{sub}}}/2 \).

Minimal supply voltage, according to [7] is \( V_{dd_{\text{min}}}=3\phi_i=78 \) mV. For \( V_{dd_{\text{sub}}}>3\phi_i \), the \( I_d(V_{gs}, V_{dd}) \) characteristic has both saturated and non-saturated areas, which is necessary for satisfying the quality of digital circuit characteristic \( V_c(V_i) \). However, logic circuits can operate even at \( V_{dd_{\text{op}}}<3\phi_i \). Thus, for example, some authors [9] state constraints \( V_{dd_{\text{op}}}>57 \) mV, while others [10] claim that \( V_{dd_{\text{op}}}>48 \) mV.

As in strong inversion regime, threshold voltage \( V_{T_{\text{sub}}} \) and maximal current \( I_{dd_{\text{sub}}} \) in the sub-threshold regime both depend on nMOS and pMOS transistor transfer geometry (Figure 3), except that \( I_{dd_{\text{sub}}} = (W_n/W_p)^{1/2} \) and \( V_{T_{\text{sub}}} \approx (W_n/W_p)^{1/2} \). where \( W_n \) and \( W_p \) are the channel widths of nMOS and pMOS transistors, respectively.

Considering the behavior analogy and CMOS inverter characteristics in the weak and strong inversion regime, there is an analogy even at synthesis of more complex circuits. In both regimes, more complex digital circuits consist of dual nMOS and pMOS transistor networks (Figure 4). Duality implies that a serial connection of pMOS transistors is corresponding to a parallel connection of nMOS transistors and vice versa.

In both regimes, logic circuit transfer characteristic depends on the number of inputs and number of active inputs [8]. Figure 5a shows the transfer characteristics of NOR3 logic circuit with all inputs activated, and when the activated input is the one applied to the gate of a pMOS transistor whose source is connected on a power-supply line \( V_{dd} \).
II. CMOS CIRCUIT ROBUSTNESS

There are four main sources of static current in CMOS circuits:

- Tunneling current through the gate ($I_{\text{tun}}$),
- Sub-threshold drain current ($I_{\text{sub}}$),
- Inverse polarized $p$-$n$ junction current ($I_{\text{DOS}}$),
- Hot charge carrier injection gate current ($I_{\text{H}}$).

The first three components have dominant influence on CMOS circuit static consumption level.

Scaling of the dimensions of MOS transistors decreases oxide thickness below the gate ($t_{\text{ox}}$). Therefore, the electric field through gate oxide increases, which leads to the tunneling effect of charge carriers from gate to substrate or from substrate to gate. The gate current has four components: gate-channel ($I_{\text{gc}}$), gate-drain ($I_{\text{gd}}$), gate-source ($I_{\text{gs}}$) and gate-base ($I_{\text{gb}}$) (Fig. 6). The total gate current is:

$$I_g = I_{\text{gd}} + I_{\text{gb}} + I_{\text{gs}} + I_{\text{gc}}.$$  \hspace{1cm} (9)

Gate currents depend on supply voltage $V_{dd}$ and on the employed technology (Table I) [11]. Thus, for example, when increasing the supply voltage level from $V_{dd}=0.2$ V to $V_{dd}=1.2$ V, the gate current increases from $I_g \approx 1.2$ nA to $I_g \approx 1.7$ µA. The increase ratio is approximately $1.4 \cdot 10^3$ times. When reducing the transistor dimensions, gate current increases as well. For nMOS transistor, according to Table I, that increase for 45 nm in regard to 65 nm CMOS technology, depending on $V_{dd}$, is approximately 7 (at $V_{dd}=1.2$ V) to 14 (at $V_{dd}=0.2$ V) times.

<table>
<thead>
<tr>
<th>$V_{dd}$ [V]</th>
<th>45 nm tech. $I_g$</th>
<th>65 nm tech. $I_g$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2</td>
<td>1.1996 nA</td>
<td>85.506 µA</td>
</tr>
<tr>
<td>0.4</td>
<td>14.258 nA</td>
<td>1.2376 pA</td>
</tr>
<tr>
<td>0.6</td>
<td>66.954 nA</td>
<td>6.5488 nA</td>
</tr>
<tr>
<td>0.8</td>
<td>225.97 nA</td>
<td>25.244 nA</td>
</tr>
<tr>
<td>1.0</td>
<td>647.38 nA</td>
<td>82.378 nA</td>
</tr>
<tr>
<td>1.2</td>
<td>1.6811 µA</td>
<td>243.21 nA</td>
</tr>
</tbody>
</table>

The nMOS transistor leakage current is greater than in pMOS, because the probability of holes tunneling is greater than the probability of electrons tunneling through the gate oxide. That increase, depending on supply voltage is 40 times [11].

The sub-threshold leakage current is a cutoff transistor ($V_{gs}=0$) drain to source current (Figure 7) and it is given as:
where $\eta$ is the DIBL (Drain-Induced Barrier Lowering) factor [9].

This current values depend on the supply voltage, the dimensions of elements (technology) and the temperature. In Table II, comparative values of gate current and sub-threshold drain current as a function of supply voltage $V_{dd}$ and temperature are given, for 45 nm technology. It is evident that the dependency of $I_g$ on $V_{dd}$ and in function of temperature dependency of $I_{sub}$ is more expressed. On the other hand, at temperature of 25°C it holds $V_{dd} \leq 0.6$ V, $I_g < I_{sub}$, while for $V_{dd} > 0.6$ V, $I_g > I_{sub}$. Thus, for example, for $V_{dd} = 1.2$ V holds that $I_g \approx 13I_{sub}$.

![Sub-threshold currents of (a) nMOS and (b) pMOS transistors in CMOS inverter](image)

**Fig. 7.** Sub-threshold currents of (a) nMOS and (b) pMOS transistors in CMOS inverter

**TABLE II.** GATE AND SUB-THRESHOLD DRAIN CURRENT OF NMOS TRANSISTOR AS A FUNCTION OF $V_{dd}$ AND TEMPERATURE

<table>
<thead>
<tr>
<th>$V_{dd}$ [V]</th>
<th>Gate current $I_g$ [nA]</th>
<th>Sub-threshold current $I_{sub}$ [$\mu$A]</th>
</tr>
</thead>
<tbody>
<tr>
<td>25°C</td>
<td>110°C</td>
<td></td>
</tr>
<tr>
<td>0.2</td>
<td>1.1996</td>
<td>1.2689</td>
</tr>
<tr>
<td>0.4</td>
<td>14.258</td>
<td>15.776</td>
</tr>
<tr>
<td>0.6</td>
<td>66.954</td>
<td>75.437</td>
</tr>
<tr>
<td>0.8</td>
<td>225.97</td>
<td>256.33</td>
</tr>
<tr>
<td>1.0</td>
<td>647.38</td>
<td>736.31</td>
</tr>
<tr>
<td>1.2</td>
<td>1681.1</td>
<td>1914.3</td>
</tr>
</tbody>
</table>

Inverse saturation current Idss of the p-n junction of a turned off transistor depends on the p-n junction surface and temperature. For 0.25 $\mu$m technology, it is between 10 and 100 pA/$\mu$m$^2$ at a 25°C temperature per area unit. In nanometer technologies, this current is less than $I_g$ and $I_{sub}$, and can be ignored.

Dynamic consumption consists of two components: switching consumption and transition (short-circuits) consumption. Switching consumption is the result of charging and discharging of a load capacitor and in both regimes is defined as:

$$P_s = P_{dssub} = C_L V_{dd}^2 f,$$

(11)

where $C_L$ is the effective output parasite capacitance, and $f$ is the switching state frequency of the CMOS logic circuit.

Transition consumption occurs due to conduction of both transistors or transistor networks (nMOS or pMOS) during switching states (transition area) (Figure 3). In strong inversion regime, transition consumption is defined with [12] and is:

$$P_{dp} = \frac{1}{3} I_{sub} (V_{dd} - 2V_t) (t_c + t_r) f,$$

(12)

where

$$I_{ddsub} = \mu_n C_{dd} \frac{W}{L} \left[ \frac{(V_{dd} - 2V_t)^2}{1 + \mu_n W/L} \right].$$

(13)

is the maximal voltage supply current in transition area, and $t_c$ and $t_r$ are the rise time and fall time input signals.

In sub-threshold regime, dissipation power of transition is defined with [8]:

$$P_{dsub} = 2\eta f I_{dsub} (t_c + t_r) f,$$

(14)

where $I_{dsub}$ is defined with (4), and $f$ is an input signal frequency.

Usually, dynamic dissipation power is calculated (estimated) in regard to clock frequency. Namely, most number of logic circuits does not change their state during every cycle of clock signal. Therefore, expressions for dynamic consumption have to be multiplied with activity factor $\alpha \leq 1$, regarding to clock frequency, so that:

$$P_{dd} = \alpha f C_L V_{dd}^2 + \alpha f I_{dd} (V_{dd} - V_t) (t_c + t_r) f,$$

(15)

and in sub-threshold regime

$$P_{dsub} = \alpha f C_L V_{dsub}^2 + \alpha f 2\eta f I_{dsub} (t_c + t_r) f.$$

Product $\alpha f$, where $f$ is the clock frequency, is the activity of the circuit indicating the number of state changes. Mostly, activity factor is $\alpha < 0.5$. It is determined empirically that static CMOS digital circuits have $\alpha = 0.1$ [13].

**IV. LOW POWER DESIGN TECHNIQUES**

Optimal project implies a compromise between operating speed and low power, which all design levels take into account [2]. In this section, we will speak about the optimal project considering the choice of transistor threshold voltage $V_t$ and system power supply voltage $V_{dd}$.

In the previous paragraph, it was shown that both static and dynamic consumptions are decreased with the reduce of $V_{dd}$.

Dynamic switching consumption in both regimes is proportional to $V_{dd}^2$. Transition consumption in the strong inversion regime is $P_{dp} \sim (V_{dd} - V_t)$, and in sub-threshold regime $P_{dsub} \sim V_{dsub}^{1/3}$. Static currents, depends on supply voltage as well (Tables I and II), so that $P_s \sim V_{dd}^n$, where $n$ is usually in the range of $1 < n < 4$. 

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Logic delay also depends on $V_{dd}$ and $V_t$. Namely, in the strong inversion regime, capacitor charging/discharging current is $I_{C} = (V_{dd} - V_t)I$ in the saturated area, and $I_{d} = (V_{dd} - V_t)I_{d}$ in the non-saturated area (Figure 8). In the sub-threshold regime that current is $I_{d} = e^{V_{dd} - V_t}$. Thus, reduction of $V_{dd}$ increases the logic delay in both regimes. In order to maintain the logic delay at lower $V_{dd}$, threshold voltage $V_t$ should be reduced. Over a long period of time, CMOS digital circuit's performance increasing scenario was conducted in the process of reduction of element's dimensions, by lowering $V_{dd}$ and $V_t$. However, reduction of $V_t$ below 200 mV leads to exponential increase of sub-threshold current as shown in (4). This may cause the static consumption to be higher than the dynamic. Consequently, it can be said that the reduction of threshold voltage is limited to approximately $V_{thm} = 200$ mV.

![Image](https://example.com/image)

**Fig. 8.** Discharge currents of capacitor $C_L$ in the strong and weak inversion regime

V. MULTI VDD/VT OPTIMIZATION TECHNIQUES

A compromise between low power and sufficient speed can be achieved using transistors with different threshold voltages. This technique is known as the multi-threshold technique or MTCMOS [14, 15]. Critical signal path is designed using logic with lower threshold voltages. Transistors with higher $V_t$ are used where delay is not critical. The second approach with the MTCMOS technique is based on the so-called gated voltage supply (Figure 9). In static states, relatively in time of logic inactivity (Standby Mode), voltage supply is turned off using transistors with high threshold voltage. Thus, the small sub-threshold current is secured, along with low static dissipation. Logic block transistors are designed with low $V_t$, so that the needed speed is preserved.

Using control “wake up” signal $SL$ (Sleep), over a pMOS transistor with high $V_t$, the connection between true $V_{dd}$ and virtual power supply $V_{app}$ is controlled. While $M_p$ is turned off, capacitor $C_b$ maintains the virtual power supply of the logic block.

Reduction of the leakage currents of inactive components can be achieved using nMOS transistors between the logic block and the ground, or with pMOS and nMOS transistors at the same time [15]. The state of the pMOS transistors is then controlled with the SL signal, and of the nMOS with the SL signal.

The ratio between the consumption and the speed of data processing is optimized using several power supplies in the same design. Logic circuits over critical delay paths are supplied with higher $V_{app}$, and circuits whose delay is not critical with lower voltage $V_{dd}$. (Figure 10). The number of voltage levels can be greater, but it turns out that the largest effect is achieved using two power supplies [16]. It should be noted that the transition from logic with $V_{dd}$ to logic with $V_{app}$ power supply is achieved using logic voltage level converters. This as well limits the number of power supply levels.

![Image](https://example.com/image)

**Fig. 9.** MTCMOS block diagram with gated voltage supply

![Image](https://example.com/image)

**Fig. 10.** Two registers connected with different delay paths

Often in the same digital system, techniques with several power supplies and several threshold voltages have been used—multi $V_{dd}$/$V_t$ techniques [16, 17]. Optimal operating point ($V_{app}$, $V_{dd}$) is determined on $V_{dd}$-$V_t$ plane with constant power consumption lines (equi-power) and speed lines (equi-speed) (Fig. 11). These lines depend on technological process and project architecture.

The choice of the optimal ($V_{app}$, $V_{dd}$) pair depends on technological process constraints. Let say that those constraints are: $V_{app}=3.3 V+10%$ and $V_{dd}=0.55 V$+0.1. The area of allowed values for these limitations is shown in Figure 11, with a larger rectangle. For all values of $V_{app}$ and $V_{dd}$, inside this rectangle, system fulfills all given specifications. In A corner, system will have the highest delay, and in B corner the highest energy consumption. Constant speed and constant consumption lines are normalized at points A and B by normalization factors $k_s$ and $k_p$, respectively. Based on that, we determine the influence

of position changes and the rectangle size in $V_{dd}/V_t$ plane, onto consumption and system speed. For example, smaller rectangle on Figure 11 is defined with constraints $V_{dd}=2.1\,\text{V} \pm 5\%$ and $V_t=0.18\,\text{V} \pm 0.05$, and consumption is 60% ($k_p=0.4$) lower for the same operating speed ($k_v=1$).

![Image](ETASR - Engineering, Technology & Applied Science Research Vol. 3, No. 6, 2013, 552-561)

**Fig. 11.** $V_{dd}/V_t$ plane with constant power consumption and delay lines

From all possible $V_{dd}/V_t$ combinations that meet given time constraints, only one combination $(V_{ddopt}, V_{top})$ guarantees minimal consumption. Shuster et al. [18] proposed an equation, based on the transistor alpha model, for the calculation of total system consumption with the optimal $(V_{ddopt}, V_{top})$ pair. Nevertheless, it should be stated that the continual change of $V_{ddopt}$ and $V_{top}$ is impractical. Designers are mostly allowed to choose between several discrete $(V_{ddopt}, V_{top})$ values. By applying the multi $V_{dd}$ technique, dynamic consumption can be reduced from 10%, up to 50%, whereas by applying the multi $V_t$ technique, static consumption can be reduced for 50%, even up to 80% [3]. In [16], the optimal ratio between $V_{dd}$ and $V_t$ is given (Table III).

**TABLE III.** **OPTIMAL RATIO OF $V_{dd}$ AND $V_t$ CONSIDERING CONSUMPTION**

<table>
<thead>
<tr>
<th>$V_{dd}, i=1,2,3,4$, $V_{t}=const$</th>
<th>$V_{dd}$, $i=1,2,3,4$, $V_{t}=const$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$(V_{aa}, V_{ab})$: $V_{aa}=0.5 + 0.5 V_t$</td>
<td>$(V_{aa}, V_{ab})$: $V_{aa}=0.5 + 0.5 V_t$</td>
</tr>
<tr>
<td>$(V_{ab}, V_{ac}, V_{ad})$: $V_{ab} = 0.6 + 0.4 V_t$</td>
<td>$(V_{ab}, V_{ac}, V_{ad})$: $V_{ab} = 0.6 + 0.4 V_t$</td>
</tr>
<tr>
<td>$(V_{ac}, V_{ad}, V_{ae}, V_{af})$: $V_{ac} = 0.7 + 0.3 V_t$</td>
<td>$(V_{ac}, V_{ad}, V_{ae}, V_{af})$: $V_{ac} = 0.7 + 0.3 V_t$</td>
</tr>
</tbody>
</table>

**VI. CMOS LOW POWER TOPOLOGIES**

Standard CMOS combinational logic demands a CMOS transistor pair per every input. However, various alternative topologies with the lower number of transistors have been developed. Besides, the increase of scale of function integration in VLSI integrated circuit, has led to a reduce of consumption or increase of speed at the same consumption level.

Among the first alternative CMOS digital logics is the transmission-gate logic. Unlike standard logic where the basic cell is the inverter, in transmission-gate logic, the basic cell is the transmission gate. While in standard logic circuits, output signals are separated from the inputs, here the input signal is transferred to the output via the transfer gate. Figure 12 shows a 2/1 multiplexer (2/1 MUX) in transmission-gate logic. Since the complementary signals are needed for transmission gate control, inverters are integral part of the network as well. The 2/1 MUX in Figure 12 consists of only three CMOS transistor pairs, while standard logic needs seven pairs.

![Image](ETASR - Engineering, Technology & Applied Science Research Vol. 3, No. 6, 2013, 552-561)

**Fig. 12.** MUX 2/1 in transmission-gate logic

Transmission gate logic can be additionally simplified by applying signals $b$ and $\bar{b}$ to the inverter power line as in the example of XOR and XNOR circuit synthesis shown in Figure 13. The inverters with the $(M_n, M_p)$ transistor pair are powered by $b$ and $\bar{b}$ signals.

In the synthesis of logical functions in transmission-gate logic, it must be taken into account that between the output and at least one input, a contour of small resistance exists. Otherwise, output would be in the state of high impedance with the undefined logic level.

![Image](ETASR - Engineering, Technology & Applied Science Research Vol. 3, No. 6, 2013, 552-561)

**Fig. 13.** (a) XOR and (b) XNOR circuits

As a transmission gate, instead of a CMOS pair, only nMOS transistors can be used (Fig. 14). The number of transistors is halved and the static consumption and the parasite
capacitance are reduced as well, which significantly increases the scale of function integration in a VLSI circuit.

![Figure 14. MUX 4/1 in pass-transistor nMOS logic with true and complementary output](image)

The problem with the nMOS pass-transistor logic is that the maximal voltage variation on one nMOS transistor is \( V_{dd} - V_{th} \) and lower, for threshold voltage \( V_{th} \) comparing to the CMOS transmission gate. That limits the number of serial transistors. Therefore, nMOS transistors with very low (NTL - Non Threshold Logic) or zero threshold voltage (ZTT - Zero Threshold Logic) have been used. The problem of mentioned logics lies in the low noise immunity.

Reduction of logic amplitude in nMOS transmission-gate logic is especially a problem when nMOS network ends with an inverter. That problem can be solved using a pMOS transistor \( M_p \) as shown in Figure 16. When \( z = 0 \), \( M_p \) is on and maintains the value of nMOS network output voltage at \( V_{dd} \).

Low threshold transistors are used in the so-called CPL (Complementary Pass-Transistor Logic). This logic consists of two nMOS transistor networks with common control and complementary transfer signals (Figure 15).

PPL (Push-pull Pass-transistor Logic) [19] also have two transistor networks: one nMOS and the other pMOS (Figure 16). The control signals are common, and inputs are complementary. Output logic levels have been restored to \( V_{dd} \) and 0 by transistors \( M_n \) and \( M_p \), respectively.

Table IV shows full adder comparative characteristics using different logics, implemented in 0.8 \( \mu m \) technology at \( V_{dd}=3.3 \) V. Although pMOS transistors are slower than nMOS, logic delay of PPL is approximately like CPL, but the consumption is significantly lower.

<table>
<thead>
<tr>
<th>TABLE IV. FULL ADDER COMPARATIVE CHARACTERISTICS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>Logic delay [ns]</td>
</tr>
<tr>
<td>Cons. [mW/100Hz]</td>
</tr>
<tr>
<td>( P_{dc} ) (normalized)</td>
</tr>
</tbody>
</table>

Fig. 15. AND/NAND (a), OR/NOR (b) i XOR/XNOR (c) logic circuits in CPL

![Figure 16. PPL block scheme](image)

VII. ADIABATIC LOGIC

The Term “adiabatic” describes thermodynamic processes in which the amount of heat remains constant (there is no exchange of energy with the environment). Adiabatic logic in the ideal sense, designate digital circuits without loss (dissipation) of electrical energy. In practice, it denotes the logic with minimal consumption of electrical energy during the switching of states. Adiabatic switching state shifting is a charge/discharge mechanism which returns accumulated...
energy to the source inside the load capacitor using the dynamic power supply. Dynamic power supply or clocked power has a very important role in adiabatic logic, because beside power supply, it provides energy recovery.

Nowadays, there are many techniques of adiabatic logic [20-25]. Energy recovery process will be explained on the example of ECRL (Efficient Charge Recovery Logic) inverter (Figure 17). Power supply PC is with trapezoidal pulses.

In the initial state holds \( a=1 \), and the \( M_{n1} \) is conducting (\( Q=0 \)). While PC rises from 0 to \( V_{dd} \), over conductive transistor \( M_{n2} \) the output \( Q \) follows the variation of PC. When PC reaches the \( V_{dd} \) value, then it holds \( Q=1 \), and \( Q=0 \) and those conditions are valid logic states at inputs of next stage. During the fall of PC from \( V_{dd} \) to zero, the right capacitor \( C_L \) discharges over the conductive \( M_{p2} \) and PC, and therefore recovers accumulated energy to the PC supply.

More complex ECRL circuits have two complementary nMOS transistor networks with complementary excitations (Figure 18), instead of \( M_{n1} \) and \( M_{n2} \) transistors. Complementary networks are obtained by complementing input signals and switching of logic operators as a function of \( f_a \) nMOS network.

For example, \( f_a \) 2/1 multiplexer function is \( f_a = (\overline{x}a + sb) \) and the function of complementary network is \( \overline{f_a} = (s + \overline{x})(\overline{x} + \overline{a}) \) (Figure 18b).

Other adiabatic topologies should be mentioned as well: PAL (Pass-transistor Adiabatic Logic) [21], CPAL (Complementary PAL), PFAL (Positive Feedback Adiabatic Logic) [20] etc. Reduced energy consumption comparing to standard CMOS logic is around 50 to 90%.

**Fig. 17.** ECRL inverter scheme

**Fig. 18.** (a) Block scheme of complex ECRL circuit (b) with \( f_a \) and \( \overline{f_a} \) MUX2/1 network

**VIII. CONCLUSION**

To enable the design of energy-efficient digital systems, designers must take into account the electrical energy consumption through all design phases, from functional description to transistor level. The biggest energy saving (10 to 20 times) with the least time needed for consumption analysis is acquired on the system design level. In the sub-threshold regime, consumption is several orders of magnitude lower, but operating speed is lowered by nearly the same amount in comparison to the strong inversion regime. Rescaling of transistor dimensions increases gate current \( I_g \) which is very dependent on power supply. Multi \( V_r/V_{dd} \) design techniques provide the reduction of consumption to a scale of about ten percent at the same operating speed. Digital systems with two power supplies and/or two threshold voltages are optimal as well. Using two threshold voltages, static consumption can be reduced up to 80%. Alternative topologies provide larger scale of function integration per single VLSI circuit, lower consumption level and higher-speed rate. The transfer logic has the widest application in VLSI digital circuit design whereas adiabatic logic ensures the greatest energy saving (up to 90%).

**REFERENCES**


