Performance Optimization of 1-bit Full Adder Cell based on CNTFET Transistor

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Abstract—**The full adder is a key component for many digital circuits like microprocessors or digital signal processors. Its main utilization is to perform logical and arithmetic operations. This has empowered the designers to continuously optimize this circuit and ameliorate its characteristics like robustness, compactness, efficiency, and scalability. Carbon Nanotube Field Effect Transistor (CNFET) stands out as a substitute for CMOS technology for designing circuits in the present-day technology. The objective of this paper is to present an optimized 1-bit full adder design based on CNTFET transistors inspired by new CMOS full adder design [1] with enhanced performance parameters. For a power supply of 0.9V, the count of transistors is decreased to 10 and the power is almost split in two compared to the best existing CNTFET based adder. This design offers significant improvement when compared to existing designs such as C-CMOS, TFA, TGA, HPSC, 18T-FA adder, etc. Comparative data analysis shows that there is 37%, 50%, and 49% amelioration in terms of area, delay, and power delay product respectively compared to both CNTFET and CMOS based adders in existing designs. The circuit was designed in 32nm technology and simulated with HSPICE tools.**

Keywords-1-bit full adder; CNTFET; PDP; low power; HSPICE

I. INTRODUCTION

Semiconductor technologies are in a constant innovation race to create a new functionality and meet growth-up expectations. Implemented semiconductor devices for scientific, industry and consumers, are expected to offer high performance with high speed, scalability, and, especially, low power consumption. In embedded electronic products such as mobile phones, laptops and connected watches, power consumption is a key element that influences directly circuit operation. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) can't no longer comply with Moore's Law [2-3], which led to the need of finding alternative technologies. Each technology has its advantages and disadvantages. Carbon Nanotube Field Effect Transistor (CNFET) is the most promising technology with interesting advantages. It is widely adopted and has become one of the most interesting research areas [4, 5]. CNFET is flexible in overcoming challenges like ballistic transport, short channel effects, low OFF-current properties, etc. Because the complete adder circuit is indispensable in any digital product, the performance of any digital circuit can be improved by enhancing it performance. Efforts to optimize performance are continuous, efforts such as the Conventional–Complementary Metal Oxide Semiconductor [1], the Removed Single Driving Full Adder (RSD-FA) [6], the Hybrid Pass Transistor Logic with Static CMOS output drive (HPSC) [3], the 18 Transistor 1-bit Full Adder [7], the Hybrid Multi-Threshold Full Adder (HMTFA) [8], and the low power based CNTFET [9]. The implementation of these adder circuits takes place using various logic families, therefore the above mentioned adders have different advantages and disadvantages. In this paper, a new schematic with 10T transistor is proposed, inspired from the new CMOS full adder design [1]. After simulation and analysis, this design offers an interesting PDP with limited number of transistors. Table I shows the comparison results for the proposed and the existing full adder designs implemented using CNFET and CMOS based on power, delay, and power delay product parameters (PDP). The proposed full adder circuit was designed with CNFET technology simulated at 32nm with a voltage supply of +0.9V using the HSPICE tool. The model used is a Stanford nano model.

II. BACKGROUND OF CNFET

Among new technologies, CNFET is placed as one with the most potential thanks to its specific physical characteristics. It offers many advantages like quasi-ballistic transport due to high mobility, fast switching due to high carrier speed, and almost one-dimensional structure of carbon nanotube for better electrostatic control [10]. In fact, each carbon nanotube reacts as a channel contrary to MOSFET, where the entire silicon acts as a channel [11]. The mobility in n and p types of CNFET is identical and the two types of transistor transfer the same driving current. This allows the creation of a completely novel logic not possible with MOSFET transistors.

III. EXISTING ADDER DESIGNS

Many full adder designs are available in the literature. Among them, the 23T full adder cell, which is an improved version of the 18T adder block [12], combining two logics, pass-transistor and transmission gate. There are five inverter stages to have the final output (Sum) causing a longer critical path and utilizing an important number of transistors. The

logical operations are performed serially and not simultaneously. Two different blocks are used to generate the Sum and the Cout. This impacts strongly the speed of this circuit and the consumed power. Another interesting design is the hybrid full adder cell [12, 13]. Two different circuits are used to generate simultaneously the Sum and the Cout output. Two cascaded XOR/XNOR cells are used to generate the Sum signal and many inverters are required. As a result, a huge number of transistors are used and the critical path becomes very long, causing speed problem. In order to solve this issue the CNTCPL architecture was proposed [14]. Because its critical path is composed of only two pass transistors, the delay is very short. In addition, using CNTFET technology increases speed, and overcomes the inconvenience of non-full-swing nodes. Although this design solves the problem of speed, it is not an appropriate choice for low-power applications. This design suffers from many issues, such as low driving capability caused by utilization of pass-transistor logic, high transistor counts due to duplicate blocks for Sum and Cout, and finally signal integrity problem caused by cascading blocks in series, especially in high frequencies. CNTFA based on CNTFET transistor is the last studied full adder design [14]. This circuit is composed in intermediate XOR and XNOR functions and pass-transistor logic. The generated XOR/XNOR signals are used as selectors in a multiplexer-based structure at the second stage to generate Sum. Sum and output carry are generated in parallel by a pass-transistor based block. This design has multiple merits like high-speed computation and low power consumption, but when facing high load capacitors, it suffers from downfalls due to its low driving capability. As discussed above, the known full adder circuits have many disadvantages and performance optimization to follow the growing expectation is an open research topic. In this context we propose a new CNTFET full adder design trying to find a solution to some of these problems.

IV. PROPOSED FULL ADDER CIRCUIT

Inspired from the new CMOS full adder design [1] we propose a 1-bit full adder based on 10 CNTFET transistors that calculate the Sum and carry using less transistors. The Sum and carry of any full adder are achieved from the input bits including the previous stage carry. The expressions giving the relationship between the input and output bits are:

$$Sum = A \oplus B \oplus Cin \quad (1)$$

$$Carry = A.B + B.Cin + A.Cin \quad (2)$$

where A and B are the inputs, the outputs are Sum and Carry and Cin represents the carry input, if any. The proposed full adder design requires 10 transistors and consists of two XOR/XNOR gates. The implemented circuit composed of two XOR gates which are designed by using four transistors each is shown in Figure 1.

Less transistor count results to less load capacitance values and so the switching power dissipation is less in this CNTFET based full adder compared to other techniques. We are presenting the smallest full adder design in CNTFET technology (Figure 1). Transistor number reduction allowed us a considerable gain in consumption and generally in PDP. The

simulation results of the proposed full adder are presented in Figure 2. To show the amelioration done by the proposed design we compared the simulation results with the best CNTFET based adder in literature. Comparison parameters were power, delay and PDP. The mathematical calculations needed to perform this comparison are explained below.
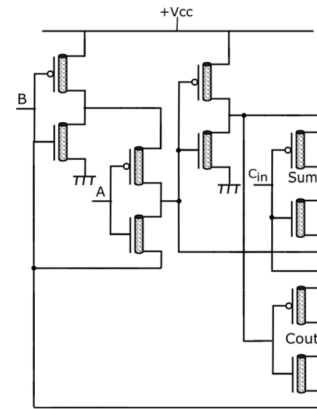

Fig. 1.   The proposed full adder cell

A. Power Consumption Calculation

PDP keeps a balance between delay and power, it is the multiplication result of the maximum delay and the average power consumption:

$$PDP = Max(Delay) \times P_{Avg} \quad (3)$$

Power average is the sum of two powers: static power and dynamic and short-circuit power [5]. Static power comes from biasing and leakage currents. The most important component of power consumption, the dynamic power, is a result of the load capacitances charging and discharging. The load capacitance, C_{load}, can be presented as a mix of a fixed capacitance, C_{fix}, and a variable capacitance, C_{var}, as follows:

$$C_{load} = C_{fix} + C_{var} \quad (4)$$

where C_{fix} is the technology-dependent due to diffusion capacitance and interconnect dependent capacitances, C_{var} is composed of the input capacitances of subsequent stages and a part of the diffusion capacitance at the gate output and can therefore be taken care of by proper transistor sizing.

$$P_{Avg} = Ids \times Vdd \times fc \times C_{load} \quad (5)$$

where Ids is the drain to source current (A), Vdd is the supply voltage (V), C_{load} is the output load capacitance (F), and fc is the clock frequency (HZ).

B. Calculation of Propagation Delay

The adder is a fundamental element in most electronic systems. That is why the optimization of its response delay affects directly the speed of the whole system. The speed of the adder response is mainly dependent on the propagation delay of the carry signal which is usually minimized by reducing the path length of the carry signal. The delay is calculated from the time that the input signal reaches ½Vdd to the time that the output signal reaches the same voltage level.

Fig. 2.   Output waveforms of the proposed full adder design

In the present design, the carry signal is generated by controlled transmission of the input carry signal and either of the input signals A or B (when A=B). As the carry signal propagates only through the single transmission gate, the carry propagation path is minimized leading to a substantial reduction in propagation delay. The delay incurred in the propagation is further reduced by efficient transistor sizing and deliberate incorporation of strong transmission gates. Based on this information, power consumption and PDP are calculated for the proposed design. In Table I, the performance of the proposed full adder is compared with existing designs [9]. The number of transistors for the proposed full adder is 10. The calculated delay is 4ps. For 0.9 Supply the power consumption is 0.073 μW and the calculated PDP is 0.592 aJ.

TABLE I.   COMPARATIVE ANALYSIS FOR NUMBER OF TRANSISTORS, DELAY, POWER, AND PDP

Full Adder	Transistor count	Power (μW)	Delay (ps)	PDP (aJ)
C-CMOS [2]	28	0.124	12.355	1.532
TGA [13]	20	0.135	10.104	1.364
CPL [17]		1.33	0.84	0.38
TFA [18]	16	0.109	11.701	1.275
HPSC [3]	26	0.095	30.654	2.912
CLRCL [15]	10	5.903	231.18	1364.65
OURS1 [4]	28	0.163	10.866	1.771
HCTG [5]	16	0.124	12.116	1.502
RSD-FA [6]	26	0.091	9.427	0.857
18T-FA [6]	18	0.088	8.93	0.785
HMTFA [7]	23	0.1216	16.909	2.056
1bFA16 [9]	16	.073	8.12	0.592
Proposed	10	0.073	4	0.295

V.   CONCLUSIONS

A novel full adder cell inspired from recent CMOS design has been presented. Although many designs have been presented recently with the aim of reducing the number of transistors, they suffer from serious problems such as PDP, and delay. Although reducing the number of transistors intrinsically leads to less area and power consumption, the other performance parameters should be taken into consideration in order to make the circuit work properly in real conditions. Simulation results prove that the proposed full adder exhibits improvement in area, delay, and PDP by approximately 37%, 50%, and 49% respectively compared to the best CNTFET-based adder found in the literature. In future work, this design can be further extended for a 32-bit full adder implementation.

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