A Novel Voltage Divider Circuit

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Abstract — **A novel analog divider is described in this paper. The circuit enables the division of a dc voltage with another dc voltage. The constant of the division is dependent upon a third dc voltage and a pair of resistors. Employing a precision source for the third dc voltage and matched resistors, an acceptable level of accuracy can be obtained.**

Keywords-sawtooth wave; integrator; comparator; analog switches; divider

I. INTRODUCTION

A common need arises for taking the ratio of two analog voltages, in many instrumentation and control applications. This operation is usually performed by a log-antilog network configuration [1]. An alternative method that has been proposed in the past is based on FET [2, 3]. The fact that a FET can be used as a voltage dependent resistor, albeit within restricted gate-to-source voltage limits, is exploited in this method. Hence, this method is useful only for small voltage levels. A different approach is to convert the input voltages to equivalent frequencies [4], take the ratio of two frequencies using conventional digital techniques, and then produce an output voltage proportional to the period of the ratio-metric signal. This method is applicable only when the numerator voltage varies within a small specified range of values. S. I. Liu and J. J. Chen developed a scheme [5] in which the analog division was performed with two current feedback op amps, one resistor and two MOSFETs. N. I. Khachab and M. Ismail developed another scheme [6] by using one op amp and eight MOSFETs. Carlos A. De La Cruz Blas and Antonio Lopez developed a scheme [7] which is based on a CMOS translinear loop using a novel biasing scheme that allows class–AB operation. Munir A. Al – Absi proposed a circuit [8] which consists of four MOSFETs biased in weak inversion.

A novel circuit for analog division using only op amps and switches is described in this paper. A feedback amplifier performs the analog division with a two-quadrant multiplier in the feedback path. Hence the divider thus obtained is a two-quadrant divider. The proposed analog divider has a better performance, even when the numerator voltage varies over a wide range.

II. CIRCUIT ANALYSIS

The circuit diagram of the proposed analog divider is shown in Figure 1. A sawtooth wave is generated by charging a capacitor at a specified rate and then rapidly discharging it with a switch. The sawtooth wave, marked as Vs in Figure 1, of peak value Vr is generated by op amps OA1, OA2 and a switch S1. Let us assume that at start, the charge and, hence, the voltage at the output terminal of OA1 is zero. Since the inverting terminal of OA1 is at virtual ground, the current through R1, namely Vr/R1 Amps, would flow through and charge the capacitor C1. During the charging of the capacitor (till the output of OA1 reaches the voltage level of Vr) the output of OA2, configured to work as comparator, will be at the LOW state and switch S1 is kept open (OFF). As soon as the output of OA1 crosses the level of Vr, say after a time period T, the output of comparator OA2 goes HIGH and the switch S1 is closed (ON). The switch S1 would then short the capacitor C1 and hence Vs would drop to zero volts. During the time period T we have:

$$Vs = \int Vr dt = \frac{Vr}{R1C1} t \qquad (1)$$

After a very short delay time Td, required for the capacitor to discharge to zero volts, the comparator output returns to LOW and switch S1 is opened, thus allowing C1 to resume charging. This cycle, therefore, repeats itself at a period (T+Td). The waveforms at cardinal points in the circuit of Figure 1 are shown in Figure 2. From (1) and the fact that at time t=T, Vs=Vr, we get T=R1C1. OA3, configured to work as comparator, compares the generated sawtooth voltage to the input voltage V1. The output of OA3 would be HIGH (Voltage level of +Vcc, being the supply voltage) till the sawtooth waveform Vs reaches the value V1 and thereafter LOW within the period T+Td. The output of OA3 is also indicated in Figure 2 as a pulse train Vm.

The ON time, Ton, of this pulse train will be:

$$Ton = \frac{V1}{Vr} T = \frac{V1}{Vr} R1C1 \qquad (2)$$

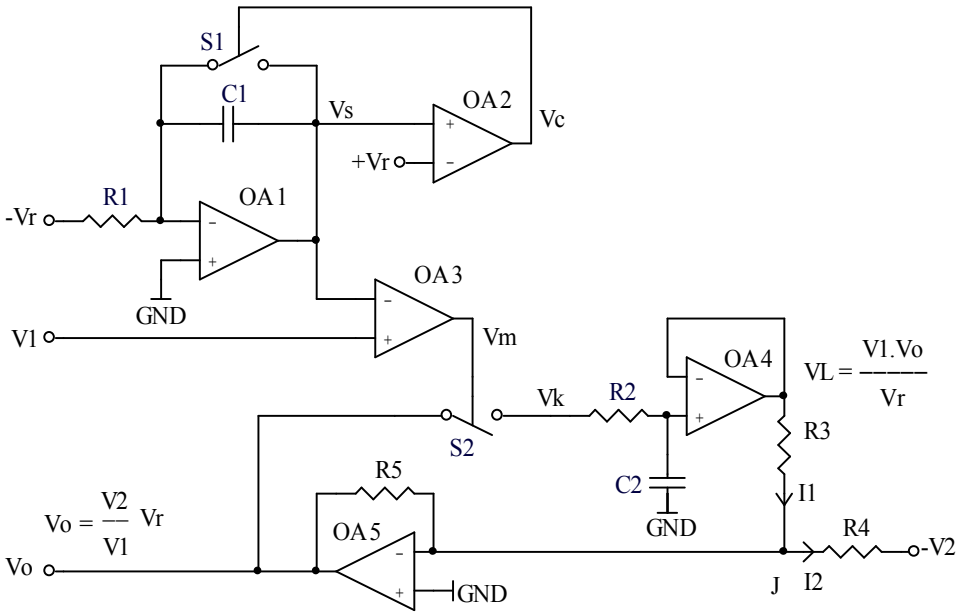

Fig. 1. Circuit diagram of proposed analog divider

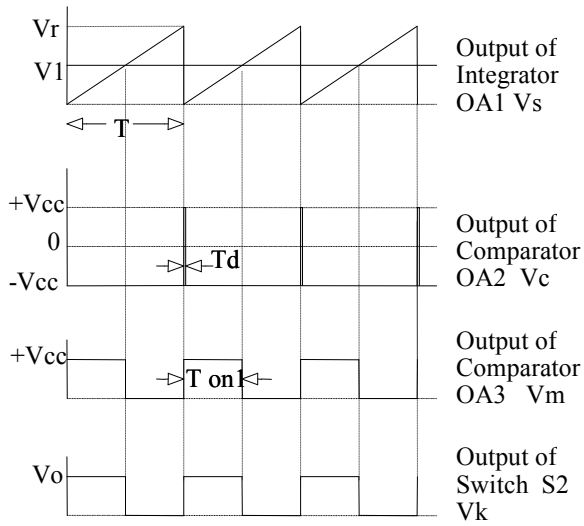

Fig. 2. Associated waveforms of Figure 1

This pulse train controls switch S2. The output of the switch would be a pulse train Vk having Ton as its ON time and amplitude of Vo. The output of S2 is given to a low pass filter realized by R2, C2 and OA4. This low pass filter extracts the average voltage of the output of switch S2. The output of OA4 will be:

$$VL = \frac{1}{T}\int_0^{Ton} Vodt\ ,\ VL = \frac{Vo}{T}Ton = \frac{V1Vo}{Vr} \qquad (3)$$

Here, the integration is done over a period T, but the actual period is (T+Td). Since T>>Td, the error introduced by the approximation would be negligibly small. OA5 sums up the output voltage of OA4 and the second input to the divider, namely, -V2. As shown in Figure 1, no input signal current can flow into the inverting terminal of OA5 which is at virtual ground. Therefore, at the junction 'J', I1=I2, where I1=VL/R3 and I2=V2/R4. If R3=R4 and R5>>R3, then VL=V2

$$\frac{V1Vo}{Vr} = V2\ ,\ Vo = \frac{V2}{V1}Vr \qquad (4)$$

III. EXPERIMENTAL RESULTS

To check the practical feasibility, the proposed circuit shown in Figure 1 was assembled with the following components values: All op amps=OP 07 ICs. Switches S1 and S2 are realized with IC CD4053. R1=200K, C1=470pF, R2=20K, C2=100uF, R3=R4=10K and R5 = 2.2M. First the divisors, namely, the input voltage V1 as well as Vr, are fixed and the numerator voltage is varied from zero to full scale. The output was measured and compared with the expected values. The results obtained are given in Table I. Then the numerator voltage V1 is set and the divisor voltage V2 is varied from zero to full scale and the results are tabulated in Table II.

As expected, when the denominator voltage kept at zero, the output Vo was at the saturation level. The results indicate practical usefulness of the proposed divider for instrumentation and control applications. It is observed that the accuracy obtained is very much dependent on the

linearity and sharpness of the sawtooth waveform. Offset voltage of all op amps will appear as an error at the output, hence offset should be eliminated by a suitable circuitry.

TABLE I. TEST RESULTS FOR V1=VR = 6V

Sl No	V2	Vo Volts Practical	Vo Volts Calculated	Error %
1	0.556	0.554	0.556	-0.36
2	1.503	1.505	1.503	0.13
3	2.514	2.513	2.514	-0.04
4	3.501	3.500	3.501	-0.03
5	4.506	4.508	4.506	0.04
6	6.012	6.006	6.012	-0.10

TABLE II. TEST RESULTS FOR V2=0.43V, VR = 3.915V

Sl No	V1	Vo Volts Practical	Vo Volts Calculated	Error %
1	0.306	5.490	5.501	0.2
2	1.002	1.673	1.680	-0.42
3	2.003	0.840	0.840	0
4	3.004	0.562	0.560	0.29
5	3.505	0.482	0.480	0.41
6	3.910	0.432	0.430	0.47

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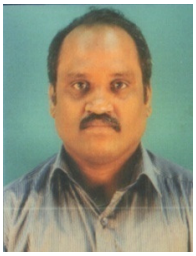

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