Realization of a Single-Phase Multilevel Inverter for Grid-Connected Photovoltaic System

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Abstract—**This paper introduces the implementation of a single-phase multilevel inverter for a grid-connected photovoltaic system. The considered topology contains a full bridge converter tied to an auxiliary circuit made of two power switches. A proportional integral (PI) current controller is established with this inverter to inject a sinusoidal current into the grid with a power factor near to unity. The studied system is tested on Matlab/Simulink and verified by experiment through a test bench comprising of a fabricated prototype and a DSP TMS320F28379D. The obtained results prove the efficiency of the inverter to maintain a direct power flow from DC sources, such as solar panels, to the grid by respecting some normalized criteria for this operation.**

Keywords-PV; multilevel inverter; PI controller; SPWM; DSP; grid connected system

I. INTRODUCTION

The use of renewable energy resources has increased considerably due to their environmental advantages compared to fossil sources. Grid connection of photovoltaic (PV) systems can't be done without using efficient power inverters and suitable control algorithms [1]. Classical inverters with two-level PWM and square wave present many problems such as high switching frequency, many harmonics, and bulky filters. Multilevel inverters appear as a good solution to overcome these problems, by developing optimal AC voltages composed at least with three levels, presenting low electromagnetic interferences, reducing the total harmonic distortion (THD) of the AC currents by using several modulation techniques and small filters, and causing low switching losses across the power switches [2, 3]. Thus, PV multilevel inverters are chosen based on the desired power rating, number of the used power switch, and manufacturing cost [2, 4]. Several control algorithms can be implemented with these inverters for the grid-connection based on different controllers. PI [5], proportional-resonant (PR) [6], predictive deadbeat (DB) [7], and hysteresis controllers [8], are the most applied in this case. This paper aims to present the test of a single-phase multilevel grid-connected inverter for a photovoltaic system, based on a full bridge converter (FBC) and an auxiliary circuit. In this work, two configurations of this inverter are presented and compared. The main objective of the control algorithm which contains a PI current controller and a phase angle detection system is to ensure sinusoidal current injection with fewer harmonics and a power factor near to unity. The PV multilevel inverter system is tested on Matlab/Simulink using a simple model of solar panels. Also, an experimental setup controlled by a DSP TMS320F28379D is used to confirm the simulation results.

II. PRESENTATION OF THE STUDIED PV MULTILEVEL INVERTER SYSTEM

The topology of the PV multilevel inverter system is shown in Figure 1. It consists of a DC source obtained from two identical solar panels coupled in series, a single-phase multilevel DC-AC converter (SPMLC), an L filter, an autotransformer for decreasing the grid voltage (Vgrid) at an adopted voltage (Vg), and the electrical grid.

A. Solar Panels

Solar panels are composed of small solar cells coupled in series, which generate DC current through the photovoltaic effect. A simplified model of a solar cell can be used, as shown in Figure 2. It's based on a current source, single diode, parallel resistance, and a series resistance [4]. The expression of the generated DC current from this model is described in (1).

$$\mathrm{I} = \mathrm{Iph} - \mathrm{Id} - \mathrm{Ish} = \mathrm{Iph} - \mathrm{I_0}\left[\exp\left(q \times \left(\frac{V+(Rs\times I)}{n\times K\times T}\right)\right) - 1\right] - \frac{V+(Rs\times I)}{Rp} \quad (1)$$

where, Iph is the photocurrent (proportional to the sunlight irradiation), I is the output current, I_0 is the reverse saturation current of the diode, q is the electron charge (1.602×10^{-19}C), K is the Boltzmann constant (1.381×10^{-23}J/K), V is the output voltage, n is the ideality factor of the diode, and T is the junction temperature in Kelvin.

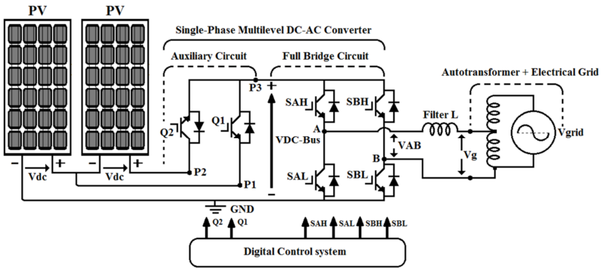

Fig. 1. Topology of the studied PV multilevel inverter system

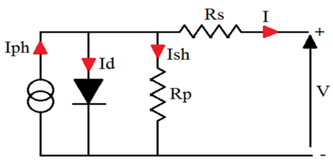

Fig. 2. Model of a solar cell

The electrical parameters of the used solar panels under the standard test conditions (STC) (1000W/m^2; 25°C) are indicated in Table I.

TABLE I. SOLAR PANEL ELECTRICAL PARAMETERS (STC)

Parameters	Values
Maximum power (Pmax)	240W
Voltage at Pmax (Vmp)	29.9V
Current at Pmax (Imp)	8.03A
Short-circuit current (Isc)	8.60A
Open-circuit voltage (Voc)	37.0V

B. Single Phase Multilevel DC-AC Converter

The suggested SPMLC is composed of an FBC circuit with four power switches (SAH, SAL, SBH, and SBL), tied to an auxiliary circuit made of two power switches (Q1 and Q2) [9]. Two configurations of this converter are studied and compared based on the obtained AC voltage (VAB) waveform.

- Configuration 1:

The FBC is connected directly to the two solar panels without using the auxiliary circuit. Thus, the voltage VAB has a waveform shape with three levels by using a simple sinusoidal pulse-width modulation method (SPWM-3L). The latter is based on comparing a triangular carrier signal (Carr A) with two reference sinusoidal signals (Ref 1A and Ref 2A) shifted by 180°, as depicted in Figure 3, and described in Table II. The rms value of the obtained voltage VAB is controlled by varying the modulation index (MI) expressed in (2), where, VcarrA and Vref1A are respectively the amplitudes of the carrier signal and the reference signal.

$$\mathrm{MI} = \frac{\mathrm{Vref1A}}{\mathrm{VcarrA}} \quad (2)$$

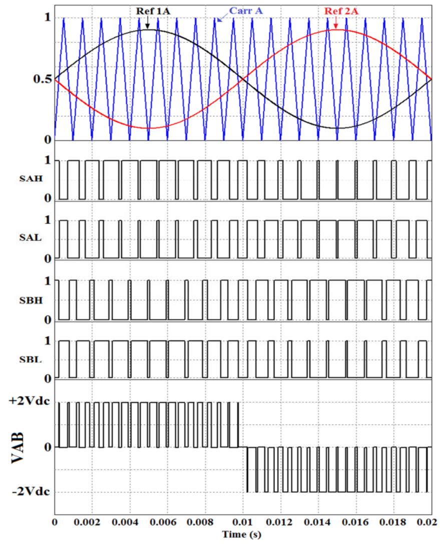

Fig. 3. SPWM-3L method for the SPMLC (three levels) with the obtained AC voltage (MI=0.8)

TABLE II. USED CONDITIONS TO SWITCH ON THE POWER SWITCHES OF THE SPMLC (THREE LEVELS)

Signals/Conditions	ON switch
(Ref 1A ≥ Carr A) = C1	SAH
(NOT C1)	SAL
(Ref 2A ≥ Carr A) = C2	SBH
(NOT C2)	SBL

- Configuration 2:

All circuitry of the SPMLC is used. In this case, the voltage VAB has a waveform shape with five levels by applying another sinusoidal pulse-width modulation method (SPWM-5L). This is based on comparing a triangular carrier signal (Carr B) with two rectified sinusoidal signals (Ref 1B and Ref 2B) with an offset equal to the amplitude of Carr B, as shown in Figure 4, and described in Table III [10]. The modulation index (MI) of this method is expressed in (3), where, VcarrB and Vref1B are respectively the amplitudes of the carrier signal and the reference signal.

$$\mathrm{MI} = \frac{\mathrm{Vref1B}}{2\times\mathrm{VcarrB}} \quad (3)$$

TABLE III. USED CONDITIONS TO SWITCH ON THE POWER SWITCHES OF THE SPMLC (FIVE LEVELS)

Signals/Conditions	ON switch
{(Ref 1B >= Carr B) AND (SBL Pulse)} OR {(Ref 1B <= Carr B) AND (SBH Pulse)}	SAH
{(Ref 1B >= Carr B) AND (SBH Pulse)} OR {(Ref 1B <= Carr B) AND (SBL Pulse)}	SAL
(Ref 1B>= Carr B) AND (Ref 2B <= Carr B)	Q1
(Ref 2B >= Carr B)	Q2

III. CONTROL TECHNIQUE OF THE SPMLC TIED TO THE GRID

The used control technique with the SPMLC connected to the grid is illustrated in Figure 5. The expected objective from this method is to transfer the power energy directly from PV sources into the grid, by respecting some standard limits which concern the interconnection between PV inverters and the electrical network [4], as described in Table IV. In addition, to provide this power flow in a correct way, the conditions described in (4) and (5) must be verified [5, 11].

$$\mathrm{VDC-Bus} > \sqrt{2} \times \mathrm{Vg(rms)} \qquad (4)$$

$$0.5 \leq \mathrm{MI} \leq 1 \qquad (5)$$

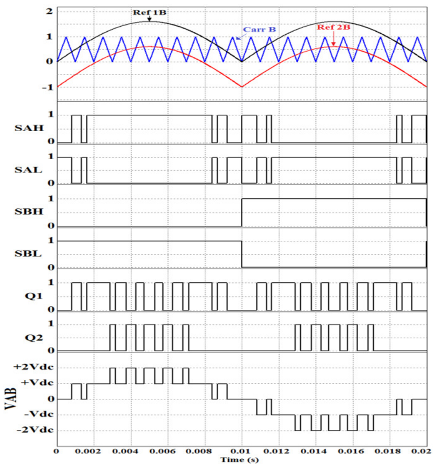

Fig. 4. SPWM-5L method for the SPMLC (five levels) with the obtained AC voltage (MI=0.8)

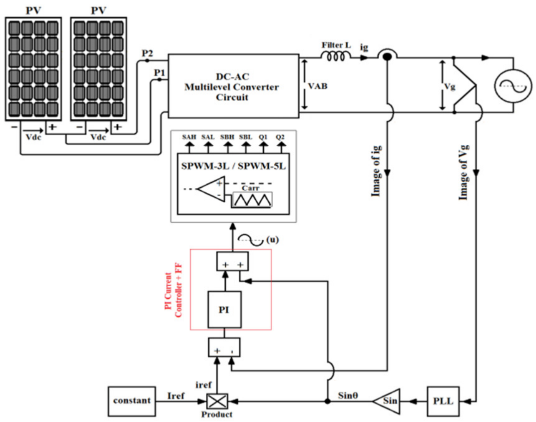

Fig. 5. The used control technique with the SPMLC tied to the gid

TABLE IV. STANDARD LIMITS DEALING WITH PV INVERTER SYSTEM INTERCONNECTIONS WITH THE ELECTRICAL NETWORK

Element	Standard limits
THD of injected current at the fundamental frequency	≤5%
Frequency range	50±1Hz
Power factor (cosφ)	>0.9

From Figure 5, the injected current ig is synchronized with the grid voltage (Vg) using a conventional phase locked loop (PLL). The latter contains three blocks, which are a phase detector (PD), a loop filter (LF), and a voltage controlled oscillator (VCO), as shown in Figure 6. Its main function is to generate a phase angle θ to get a sinusoidal signal identical to Vgrid waveform, while the used PI controller in the LF bloc is responsible for the synchronization time (settling time) [12]. In addition, the main PI current controller of the control system is used to correct the resulting error signal (ε) from the difference between the reference current (iref) and the actual injected current (ig), as described in (6), to ensure that ig is in phase with the grid voltage and operates at near-unity power factor. iref is formed with the obtained sinusoidal waveform from the PLL, and the given value of Iref which represent the amplitude. Iref is considered constant with the possibility to vary its value because the maximum power point tracking (MPPT) method is not used in this study. This PI controller is equipped with a feed-forward from the PLL to track the sinusoidal reference (iref) without steady-state error. Also, to overcome the problems caused by the integral-mode windup such as larger transient overshoots and longer settling times, anti-windups are added to this controller [5]. The obtained reference sinusoidal signal (u) from the control system is then treated in order to get the gate pulses for the power switches based on the proposed SPWM methods.

$$\varepsilon = \mathrm{iref} - \mathrm{ig} = (\mathrm{Iref} \times \mathrm{Sin}\theta) - \mathrm{ig} \qquad (6)$$

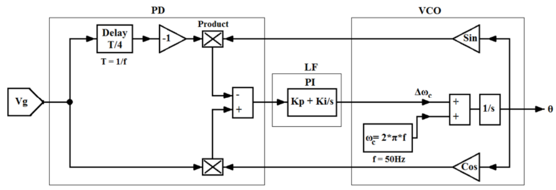

Fig. 6. The used PLL

IV. SIMULATION RESULTS

The studied PV multi-level inverter system (Figure 5) is tested on Matlab/Simulink using the model of the two identical solar panels (Table I). During simulation tests, the irradiation level is fixed at 300W/m^2, thus, the maximum PV power energy available is 140W. The grid voltage Vg is 36V rms, the grid frequency (f) is 50Hz, the value of the filter L is 30mH, and the frequency of the used carrier signals (Fcarr) is 2.5 KHz.

A. Configuration 1 Tied to the Grid

In this test, the SPMLC with three levels (SPMLC-3L) is tied to the grid using the PI current controller. The desired injected current is 1A rms (Iref=1.4). The simulation results obtained in this case are shown in Figure 7 to Figure 9.

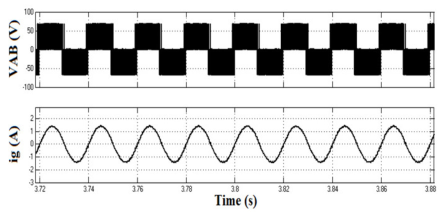

Fig. 7. The voltage VAB and the current ig from the SPMLC-3L

From these results, the mean value of Vpv in the DC-Bus is 68V (the condition described in (4) is verified), and the mean value of Ipv is 0.68A. The SPMLC delivers an output voltage VAB with three levels by using a modulation index MI=0.9 (the condition described in (5) is verified). The injected current ig is synchronized with the voltage Vg, having an rms value of 1A (the desired value), and a power factor near to unity (cosφ=0.95). Also, the computed THD of this current at the fundamental frequency (50Hz) is less than 5% (3.9%).

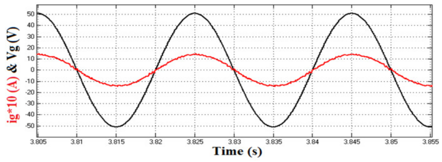

Fig. 8. The voltage Vg with the injected current ig*10 (SPMLC-3L)

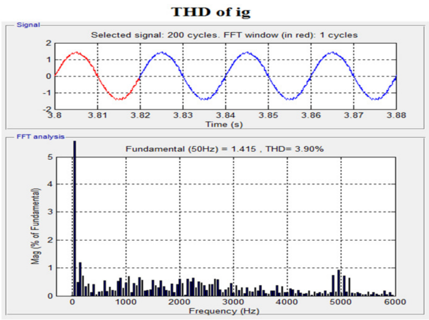

Fig. 9. THD of the injected current ig (SPMLC-3L)

B. Configuration 2 Tied to the Grid

In this second test, the SPMLC with five levels (SPMLC-5L) is also tied to the grid using the PI current controller. Two cases are discussed based on the values of Iref.

- Case 1:

The desired injected current is 1A rms (Iref=1.4). The important simulation results are depicted in Figure 10 to Figure 12.

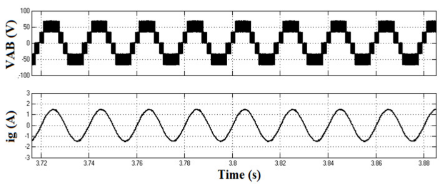

Fig. 10. The voltage VAB and the current ig from the SPMLC-5L

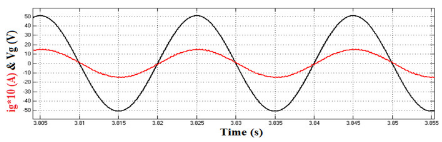

Fig. 11. The voltage Vg with the injected current ig*10 (SPMLC-5L)

From the presented results, The DC-Bus has two states which begin with 34V and ends at 68V. The mean value of the current Ipv is 0.84A. The SPMLC works with a modulation index MI=0.9 by delivering an output voltage with five levels. The injected current is synchronized with the grid voltage, having an rms value of 1A, and a power factor near unity (cosφ=0.96). The computed THD of this current at the fundamental frequency (50Hz) has decreased (2.74%) compared to the results shown previously in Figure 9.

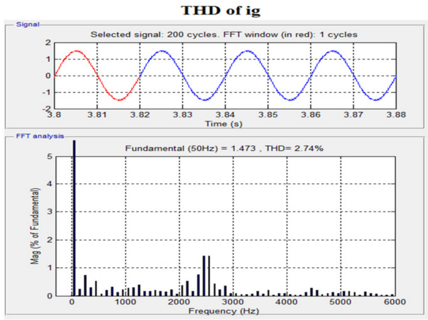

Fig. 12. THD of the injected current ig (SPMLC-5L)

- Case 2:

To test the robustness of the control method, the desired injected current is chosen now variable (similar to the effect of variable solar irradiation when using MPPT). This is done by varying the values of Iref from 1.4 (ig=1A rms) to 2.2 (ig=1.5A rms), and from 2.2 to 1.4, as depicted in Figure 13.

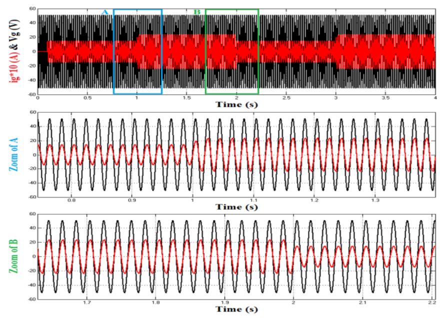

Fig. 13. The variation of the injected current ig*10 with the voltage Vg

From this result, the proposed PI controller tracks successfully the variation of the injected current without steady-state error.

V. EXPERIMENTAL RESULTS

In order to validate the tests presented in the simulation, a test bench is prepared at the laboratory using a fabricated prototype of the SPMLC, as shown in Figures 14 and 15. The two solar panels are replaced with variables stiff DC sources (0-63V/0-3A). The PI current control system is implemented using a low-cost (<50€) DSP TMS320F28379D. The experimental results are recorded using a digital oscilloscope which contains two channels for measuring (ch1 and ch4), and a current sensor with a scale of 210mv/1A rms. A measurement card consisting of Hall effect current sensors and Hall effect voltage sensors is used to measure ig and Vg. The important parameters considered practically are the same exposed previously in the simulation. Figures 16 to 18 show the experimental results for the SPMLC-3L, while Figures 19 to 23 show the experimental results for the SMPLC-5L (the used conditions are those used in the simulation tests).

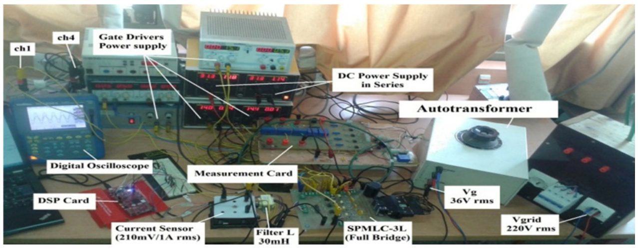

Fig. 14. The experimental test bench with the SPMLC-3L tied to the grid

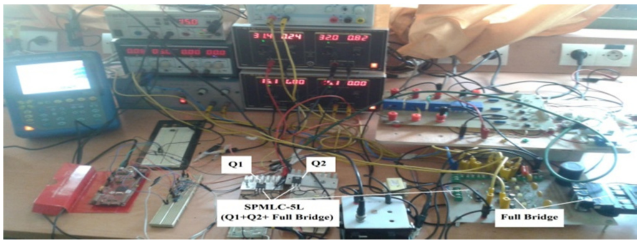

Fig. 15. The experimental test bench with the SPMLC-5L tied to the grid

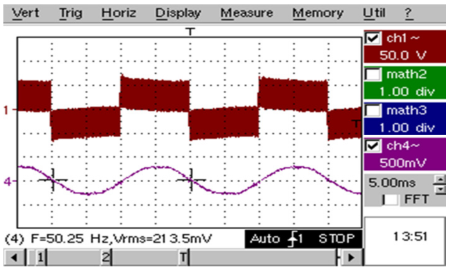

Fig. 16. The voltage VAB (ch1) and the current ig (ch4) (SPMLC-3L)

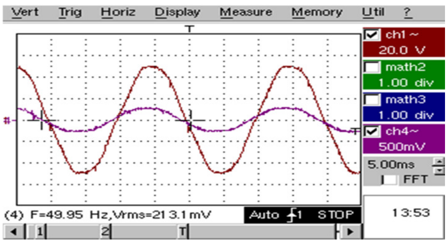

Fig. 17. The voltage Vg (ch1) and the current ig (ch4) (SPMLC-3L)

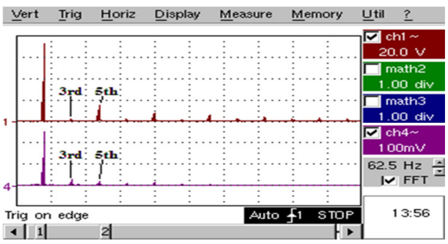

Fig. 18. FFT spectrum of VAB (ch1) and the current ig (ch4) (SPMLC-3L)

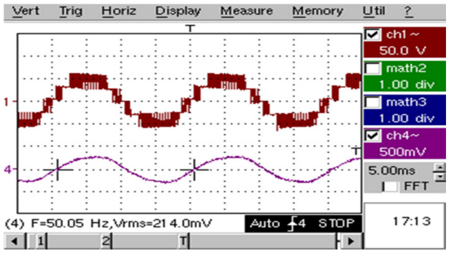

Fig. 19. The voltage VAB (ch1) and the current ig (ch4) (SPMLC-5L)

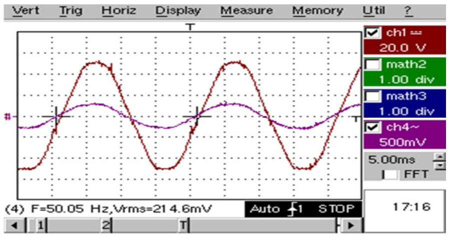

Fig. 20. The voltage Vg (ch1) and the current ig (ch4) (SPMLC-5L)

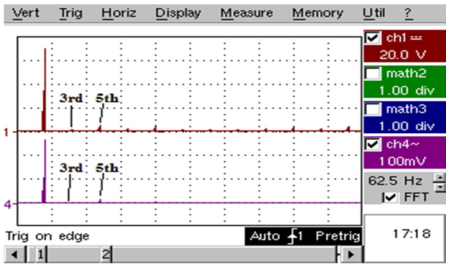

Fig. 21. FFT spectrum of VAB (ch1) and the current ig (ch4) (SPMLC-5L)

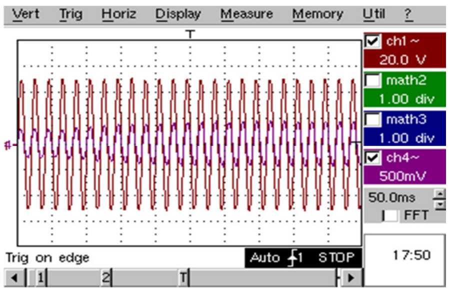

Fig. 22. The variation of the injected current ig from 1A rms to 1.5A rms (ch4) with the voltage Vg (ch1) (SPMLC-5L)

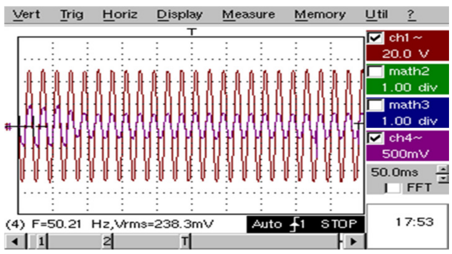

Fig. 23. The variation of the injected current ig from 1.5A rms to 1A rms (ch4) with the voltage Vg (ch1) (SPMLC-5L)

The experimental results are identical to the simulation ones. Also, the THD of the SPMLC-5L is less than that of the three-level. This confirms the utility of using multilevel inverters for the grid connection (five levels and more).

VI. CONCLUSION

This paper presented a test of a single-phase multilevel inverter tied to the grid for PV systems. Two efficient SPWM methods were used to get output AC voltage with three levels and five levels. A simple control system based on a PI controller and a conventional PLL was implemented to ensure a direct power flow into the grid. The simulation results were verified experimentally using a fabricated prototype monitored with a low-cost DSP card. The current was injected successfully from the DC source (PV) into the grid in sinusoidal form, with a power factor near to unity, a THD less than 5%, and a frequency of 50Hz. The future scope of this study is to test other controllers such as the PR controller, the use of MPPT algorithm, and increase the working voltages.

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