Comparative Assessment of Gate Drive Control Schemes in High Frequency Converter

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Abstract—**Several gate drive control schemes are simulated and the results show that the Fixed Duty ratio (FDR) can help drive synchronous rectifier buck converter (SRBC) correctly with low dead time and hence reduce body diode conduction loss. Even though FDR is prone to cross-conduction effects, the design is simple. Apart from that, Adaptive Gate Delay (AGD) and Predictive Gate Delay (PGD) control schemes have also shown high level of efficiency. However, AGD generates more losses. This makes PGD preferable in achieving a highly efficient converter of more than 82 % in spite of the advantage in FDR and AGD schemes.**

Keywords-gate drive control; high frequency; PSpice simulation; synchronous rectifier buck converter

I. INTRODUCTION

Many control schemes in gate driver for DC-DC converters have been introduced back in the 1990s. They include digital and also analog controls. In 1997, pulse based dead time, T_D compensator (PBDTC) was introduced [1] where the switching times were modified to compensate T_D so that output voltage, v_o can be properly controlled in magnitude. In addition, it can adjust symmetric Pulse Width Modulator (PWM) pulses to correct voltage distortion. This replicates the fixed delay implementation. Some other literatures have discussed different methods in details [2, 3].

On the other hand, in recent development, several analog techniques have been developed to ensure "break before make" operation. They are the Fixed "dead time" or Fixed Duty Ratio (FDR), Adaptive Gate Delay (AGD) and Predictive Gate Delay (PGD). Each of them has its own characteristics, advantages and drawbacks which provide information for the suitability and cost effective gate driver design.

A. Fixed Duty Ratio (FDR)

Fixed Duty Ratio is the first PWM controller for synchronous rectifier buck converter (SRBC) circuit. The advantage of this technique is that it has a simple control circuit with lower voltage stress [4, 5]. However, this scheme requires the T_D to be provided long enough to cover the entire applications so that no cross conduction will occur. A lengthy T_D would reduce the converter efficiency by allowing the body diode to conduct.

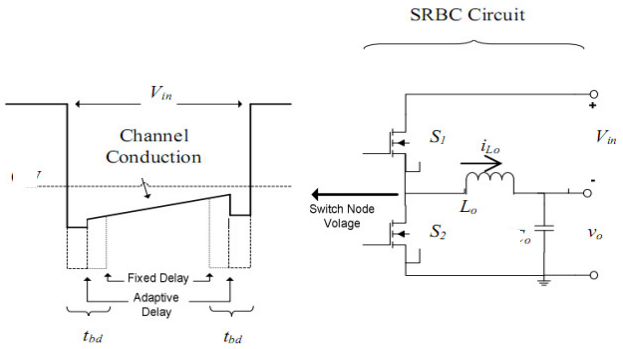

Fig. 1. Switch Node Waveform of SRBC

Figure 1 shows typical switch-node voltage waveform of SRBC. It shows the relative effects of FDR and AGD control schemes on body diode conduction time, t_{bd}. Theoretically, FDR scheme in general, produces a longer t_{bd} eventually reducing the channel conduction time. However, a precise timing control could solve this issue. During t_{bd}, the inductor current, i_{Lo} will flow from ground through the body diode of switch S_2 and L_o resulting the voltage drop across body diode which leads to the reduction in the efficiency of power conversion [6].

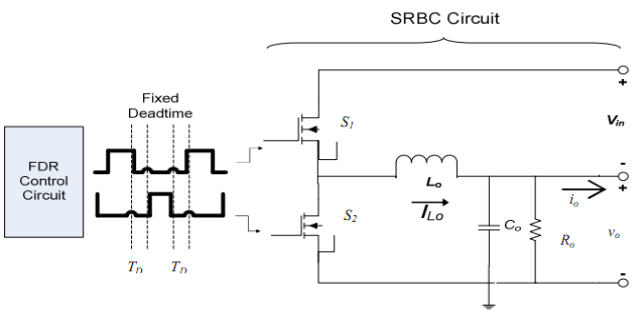

Fig. 2. Block Diagram of FDR Scheme with SRBC

Figure 2 shows the block diagram of FDR control circuit integrated with SRBC circuit. The input signal produced by the driver circuit has T_D application between switches. In addition, the efficiency of FDR technique also varies with different type of MOSFETs' ambient temperature and with lot-to-lot variation of the T_D delay during manufacturing [7].

B. Adaptive Gate Delay (AGD)

Figure 3 shows the Adaptive Gate Delay (AGD) control scheme. This second generation gate driver control scheme was introduced to overcome the limitation in the FDR. It uses a control loop that includes a digital delay line where it senses the drain to source voltage, v_{ds} of the S_2 and adjusts the digital delay line according to the amount of delay that should be applied to turn on S_2. Consequently, S_2 is turned on only when the switch node voltage equals to zero [8].

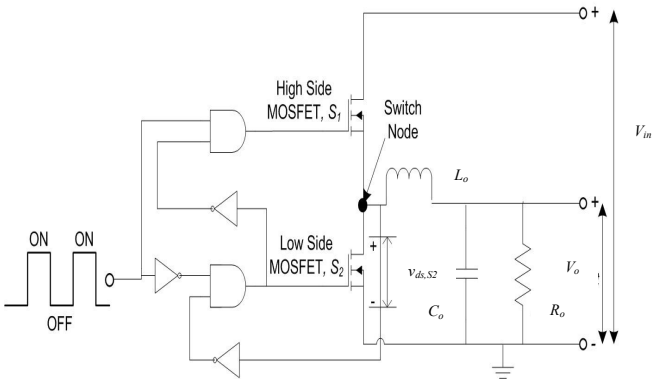

Fig. 3. Adaptive Gate Delay Control Scheme

The advantage of using this control scheme is that the adjustment of the delay can be made adaptively according to the type of MOSFET used. However, there is a disadvantage that comes from this control scheme. The variation of body diode conduction time interval may not easy to predict. This is due to the logic components used as the feedback circuit. Each of the components has its own propagation delay which may indirectly increase the T_D between the pulses.

C. Predictive Gate Delay (PGD)

Since both FDR and AGD schemes have limitations, the Predictive Gate Delay (PGD) control scheme was then introduced. It is a combination of a predictive circuit integrated with PWM where it has the ability to vary the T_D from time to time according to the feedback signal. The predictive time is shown in Figure 4. Here, the next T_D, $T_{D[n+1]}$ can be predicted and minimized based on the feedback.

PGD uses feedback loop as shown in Figure 5 in order to reduce the T_D until it reaches near zero [9]. The predictive circuit will sense a signal (it can be in the form of Voltage or Current) from the SRBC Circuit.

Table I shows the summary of all three gate driver control schemes for SRBC circuits. Even though FDR is not suitable, it has the simplest configuration and easy to drive the SRBC. The only issue is that the T_D has to be provided longer. However, this is not true since simulation results proved otherwise [10], the details of which are presented in Results and Discussions section. The data in the table gives the advantages and disadvantages of different control schemes so that the choice of the design can easily be made based on cost, component count and simplicity.

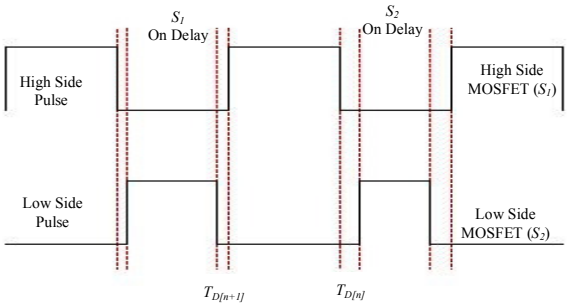

Fig. 4. Predictive Timing

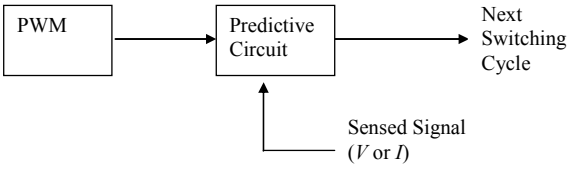

Fig. 5. PGD Scheme Block Diagram

TABLE I. ADVANTAGES AND DISADVANTAGES OF GATE DRIVE CONTROL SCHEMES

Fixed Duty Ratio	Adaptive Gate Delay	Predictive Gate Delay
- constant, pre-set delays for turn-off to turn-on intervals - simple in design - efficiency varies with MOSFET types and ambient temperature - Need to make delay long enough to cover entire application.	- variable delays based on volatage sensed on current switching cycle - uses state information from power stage to control turn-on of two gate drivers and set T_D - increases body diode conduction time caused by delay in cross coupling loops - unable to compensate for delay to charge MOSFET gate to threshold level - difficult to determine whether S_2 is off	- uses information from current switching cycle to adjust delays to be used in next cycle - can prevent body diode from being forward biased and hence cross conduction - increases power savings when MOSFET is turned on - minimizes reverse recovery loss in S_1 body diode. - tight layout regulation requirement

II. METHODOLOGY

In this part of work, dual-channel function generators are again used to fix the pulse widths and T_D of Q_1 to Q_4 switches for Fixed Duty Ratio (FDR) scheme to proposed dual-channel Resonant Gate Drive (RGD) circuit as shown in Figure 6 [10]. On the other hand, a set of combinational discrete components and transistor-transistor logic (TTL) gates are employed for the generation of Adaptive Gate Delay (AGD) and Predictive Gate

Delay (PGD) schemes. All three schemes are compared to determine the effectiveness in terms of switching loss, output power distribution, body diode conduction loss and efficiency of the converter. Figure 7 and Figure 8 show the proposed AGD and PGD schemes respectively.

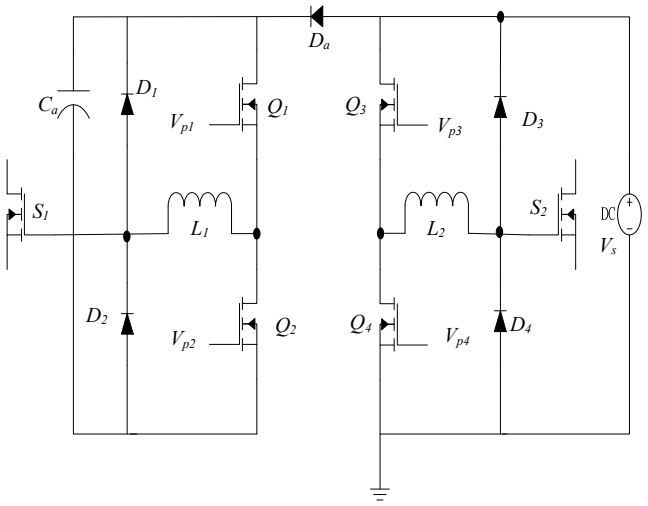

Fig. 6. Proposed Dual-Channel Gate Drive Circuit

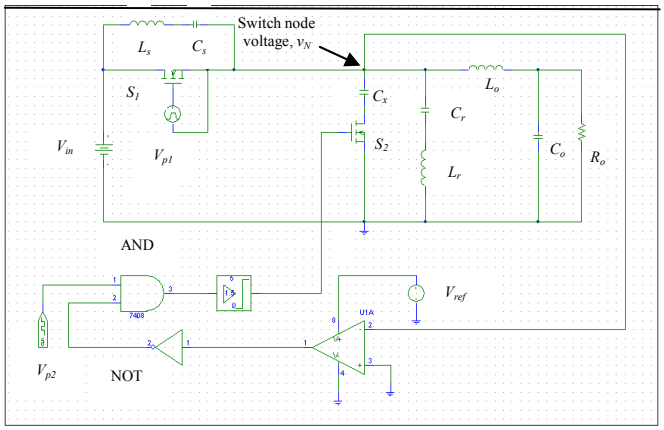

Fig. 7. Proposed Adaptive Gate Delay Scheme

The digital control block is included in the AGD scheme for the proposed SRBC circuit shown in Figure 7. In this scheme, S_1 is applied with a fixed PWM signal. S_2 switch is actually controlled by the scheme. Here, the node switch voltage is first captured and compared with the reference voltage, V_{ref}. The digital clock will then be fed to the AND gate so that when the clock triggers with input 1, S_2 switch will not turn on until node voltage is zero. The T_D is measured along side with the body diode conduction time of S_2. As a result, the conduction loss, P_{COND}, body diode conduction loss, P_{BD} and total switching loss, P_{sw} can be calculated. The digital delay line settings are shown in Table II.

TABLE II. DIGITAL DELAY LINE SETTINGS

Parameters	Value
Delay (ns)	340
On Time (ns)	645
Off Time (ns)	355
Start value	0
Opposite Value	1

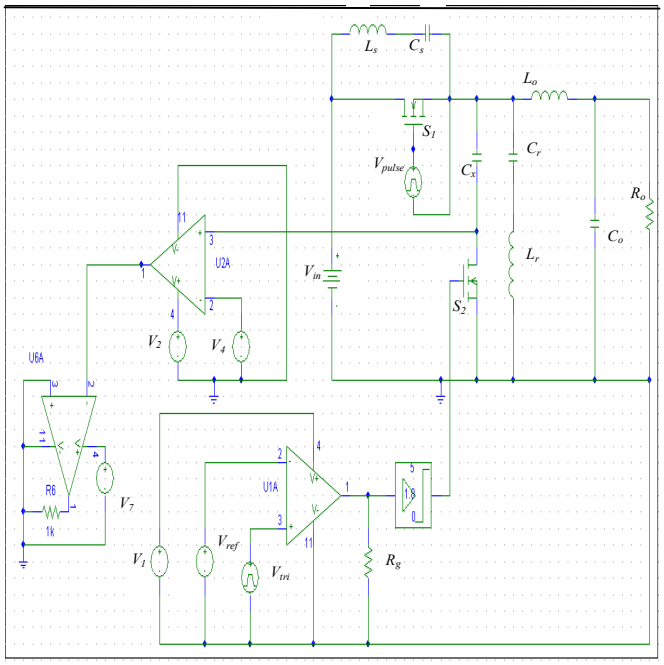

Fig. 8. Proposed Predictive Gate Delay Scheme

On the other hand, in PGD control scheme as shown in Fig 8, the PWM technique using comparator is used where an equal pulse width will be generated from the comparison between the triangular waveform, V_{tri} and a reference voltage, V_{ref}. The comparator will produce an output voltage each time V_{tri} goes above V_{ref}. In this work, the pulse width will be varied by adjusting V_{ref} in between 0.2 V and 0.8 V, to find out the capability of T_D reduction in SRBC circuit.

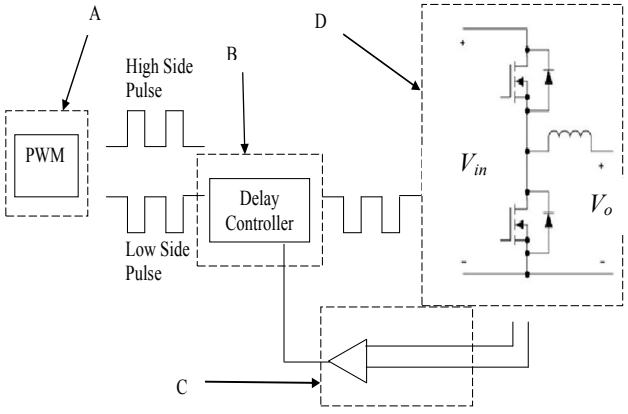

Fig. 9. Block Diagram of PGD Control Scheme

The Block Diagram of the PGD is shown in Figure 9. Note that it is constructed from several circuits constituting PWM circuit (A), Delay Controller Circuit (B), Circuit to sense the body diode conduction (C), and SRBC Circuit (D). The PWM circuit (A) will generate the pulse that is used to turn on and off the MOSFET. The high side pulse will directly be used to drive S_1. The low side pulse will be the input of the delay controller (B) before it drives the S_2. Circuit (C) will perform the feedback operation and generate output signal to the delay controller. The operating details of block B and C are described below.

Delay Controller Circuit

The delay controller circuit will adjust the low side pulse before the output drives the S_2. The adjustment is based on the prediction concept where the width of the pulse will be adjusted by the controller according to the feedback signal it receives. From Figure 10, the *D[n]* pulse is currently turned on the S_2. During this turn-on period, the feedback circuit will sense the conduction at S_2 due to the inductive load and it will generate a signal to the Delay Controller. Based on this signal, the controller will make an adjustment for the next pulse, *D[n+1]* so that the dead time, $T_{D[n+1]}$ for next switching cycle can be minimized while preventing the cross conduction.

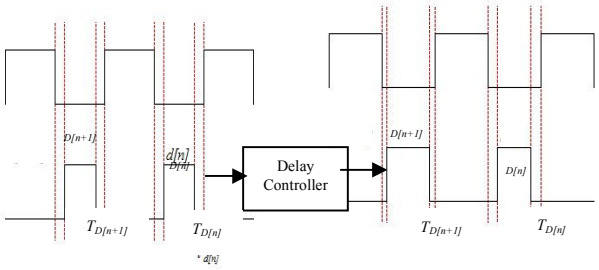

Fig. 10. Adjustment of Pulse Width Using Delay Controller

The adjustment made by the controller can be either to maximize or minimize the pulse width. Note that the dead time for $T_{D[n+1]}$ is adjusted by the delay controller. The adjustment of the pulse width can be done by varying the reference voltage, V_{ref}. So, the delay controller will be fed to the reference voltage. It has the ability to vary the reference voltage according to the received input from the feedback circuit. Figure 11 illustrates how the pulse width can be adjusted based on the feedback circuit.

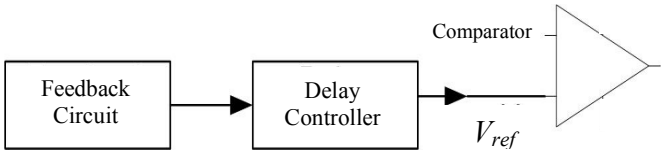

Fig. 11. Operation of Delay Controller

This is a circuit which the feedback operation is performed. The output generated from this circuit will be used as the input for the Delay Controller. During the high side pulse transition from HIGH to LOW, the comparator will sense the v_{ds} of S_2. If body diode conduction is detected, the comparator will generate HIGH output and the delay controller will reduce the delay of low side pulse for the next switching cycle. If the comparator output generates a LOW output, the delay controller will increase the delay for the next switching cycle of S_2. As long as the SRBC operates, this shifting process will continuously occur to avoid the cross conduction while ensuring the T_D delay introduced is small.

The feedback circuit will be received by the delay controller. Based on the signal received, the delay controller will adjust the V_{ref}. Since the width of the pulse generated depends on the comparison between the V_{tri} and V_{ref}, the variation in V_{ref} will change the T_D between the pulses accordingly. The parameter setting for V_{tri} and V_{ref} are given in Table III and Table IV respectively. Using the required frequency of 1 MHz, the frequency of the V_{tri} must also be same. As previously mentioned, the duty ratio, D of S_1 is determined to be 20 %.

TABLE III. PARAMETER SETTINGS FOR V_{tri}

Parameters	Value
Max Voltage, V_1	0
Min Voltage, V_0	1
Rise Time, t_r	0.5 µs
Fall Time, t_f	0.5 µs

TABLE IV. PARAMETER SETTINGS FOR V_{pulse}

Parameters	Value
Max Voltage, V_1	5 V
Min Voltage, V_0	0 V
Rise Time, t_r	5 ns
Fall Time, t_f	5 ns
Time Delay, t_d	893 ns
Pulse Width, PW	200 ns
Time Taken for a Complete Cycle, PER	1 µs

The steady-state simulation analysis is repeated with different V_{ref} values in order to investigate the effect in T_D on SRBC circuit's performance. The study on the $P_{COND} - P_{BD}$ and $T_D - t_{bd}$ relationships with respect to V_{ref} are also carried out in addition to switching related losses in the converter.

III. RESULTS AND DISCUSSIONS

FDR, AGD and PGD control schemes are investigated to determine the feasibility in the reduction of SRBC's switching loss. In FDR scheme, the proposed dual-channel gate driver is applied directly to the converter. As for AGD and PGD control schemes, each of them is configured to connect the gate terminals of Q_4 and S_2 respectively. Then, the simulated results are compared and analyzed.

A. Comparison between FDR and AGD Control Schemes

Table V shows the comparison in the analysis of FDR and AGD circuit operations. The initial study concentrates on the AGD scheme which was applied directly to the gate terminal of Q_4 (AGD-Q_4) in the proposed RGD circuit as shown in Figure 12 below. It is found that the implementation of AGD-Q_4 does not show significant improvement in SRBC except for the V_o compared to FDR. When AGD-Q_4 is used, this adds up the S_2 body diode conduction time caused by the delay in cross coupling loops during T_D detections in Q_3-Q_4 and S_1-S_2. As a result, S_2 will take a longer time to conduct. Moreover, the proposed AGD-Q_4 scheme requires a precise control on gate charge compensation delay of the switch. Otherwise, this may result in higher switching loss as measured of 2.52 W, which is more than 7 % higher than FDR.

The switching power loss is measured to be higher in AGD-S_2 as shown in Figure 7 compared to AGD-Q_4 (Figure 12). This is due to the impact of C_x in the converter which prolongs the detection of T_D by the controller and hence reduces the efficiency. When comparing with FDR, their switching losses have increased by more than 7 % and 24 % respectively.

Therefore, this clearly indicates that using the proposed dual-channel RGD may help solve issues related to T_D, reduce conduction loss to 68.30 mW and hence switching loss. In other words, by applying the digital delay control directly to S_2 will not give much advantage in converter performance. This is the remarkable finding where the proposed stand-alone dual-channel RGD network can generate better loss savings in the converter.

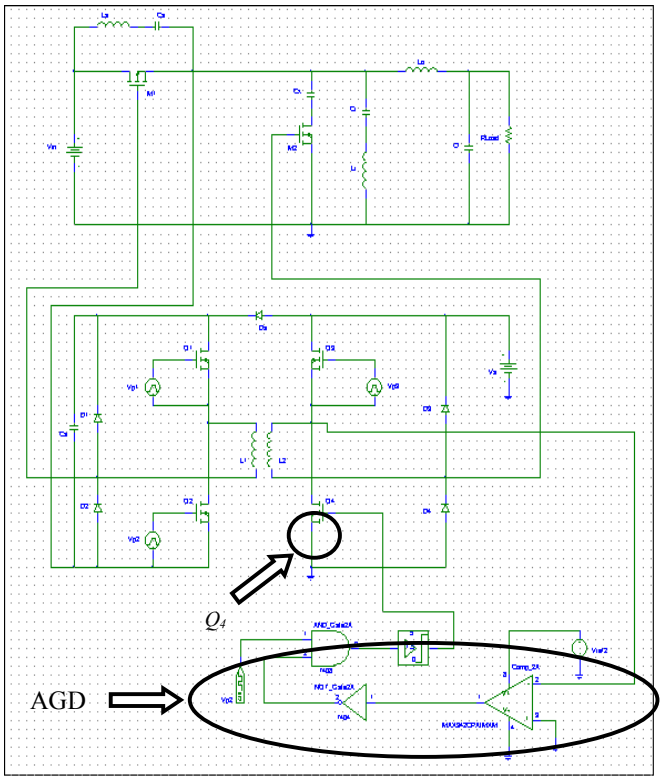

Fig. 12. RGD Circuit with AGD Control at Q_4 Switch

TABLE V. FDR, AGD-Q_4 AND AGD-S_2 ANALYSIS FOR D = 20 %

Parameters Analyzed	FDR	AGD-Q_4	% Δ to FDR	AGD-S_2	% Δ to FDR
V_o (V)	10.18	10.41	2.21	10.27	0.88
I_{Lo} (A)	1.51	1.27	15.89	1.28	15.23
t_{bd} (ns)	24	27	11.11	28	14.28
P_{COND} (mW)	68.30	86.90	21.40	87.40	21.85
P_{BD} (mW)	25.73	26.11	1.46	28.62	10.10
P_{sw} (W)	2.33	2.52	7.54	3.09	24.6

B. FDR and PGD Control Schemes

The simulation of PGD control scheme is carried out based on the variation of V_{ref} as shown in Figure 8 and it is applied directly to the gate of S_2 (PGD-S_2) in the proposed SRBC circuit through delay controller. The simulation data are presented in Table VI. From the variation of V_{ref} in the PGD-S_2 control block, the SRBC switching losses in both S_1 and S_2 are measured. As V_{ref} is decreased from 0.8 V to 0.27 V, all parameter values except i_{Lo} reduces with respect to T_D. Then once V_{ref} is below 0.27 V, the results are no longer valid since T_D is negative. It is also found that low switching losses lie between 0.27 V and 0.3 V. If V_{ref} is applied with less than 0.27 V, the pulses will overlap each other and lead to cross-conduction. A high V_{ref} yields a greater output voltage which is favorable in the design but the body diode conduction loss will increase resulting in high total switching loss in the circuit.

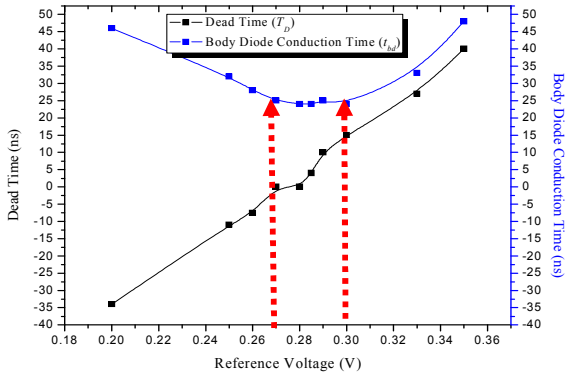

Fig. 13. Relationship between T_D and t_{bd} Vs V_{ref}

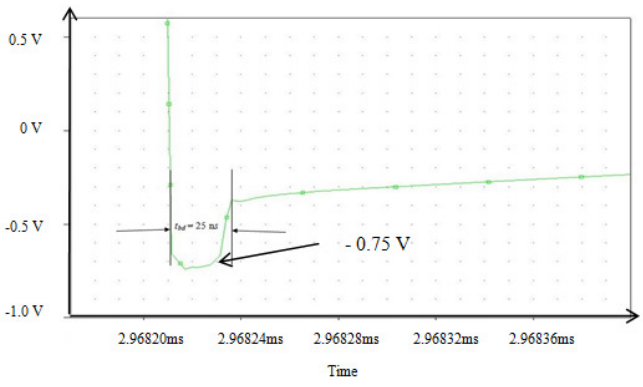

Fig. 14. Body Diode Conduction Time at V_{ref} of 0.29 V

TABLE VI. SWITCHING LOSS MEASUREMENT ADOPTING PGD-S_2 CONTROL SCHEME FOR D = 20 %

V_{ref} (V)	V_o (V)	I_{Lo} (A)	T_D (ns)	t_{bd} (ns)	P_{COND} (mW)	P_{BD} (mW)	$P_{sw,S1}$ (W)	$P_{sw,S2}$ (W)	$P_{sw,Total}$ (W)
0.8	11.60	1.12	260	350	103.90	109.0	1.64	1.03	2.88
0.6	11.23	1.25	170	220	115.65	77.0	1.96	1.42	3.34
0.4	10.23	1.31	66	82.5	92.51	54.9	1.42	1.25	2.82
0.35	10.41	1.48	40	48	81.15	48.8	1.61	1.20	2.94
0.33	10.35	1.50	27	33	71.24	36.8	1.56	1.15	2.82
0.3	10.24	1.52	15	24	68.27	24.6	1.16	1.10	2.35
0.29	10.22	1.53	10	25	67.27	24.0	1.17	1.09	2.35
0.285	10.11	1.54	4	24	62.43	23.5	1.15	1.10	2.33
0.28	10.07	1.56	0	24	61.89	23.7	1.18	1.11	2.38
0.27	10.02	1.58	0	27	60.25	23.2	1.20	1.15	2.43
0.26	10.95	1.29	-7.5	28	59.57	28.5	1.28	1.90	3.26
0.25	11.89	0.98	-11	32	66.93	30.7	1.32	2.35	3.76
0.2	12.38	0.64	-34	46	71.68	33.1	1.56	3.10	4.76

Figure 13 explains that the t_{bd} increases linearly with T_D starting from V_{ref} at 0.27 V. The faster free-wheeling i_{Lo} flows into the body diodes during T_D, the lower power loss in the converter will be. For instance, at V_{ref} = 0.29 V, the t_{bd} is measured 25 ns with - 0.75 V overshoot indicating the duration of on-state conduction of body diode as shown in Figure 14. Therefore, t_{bd} has to be minimized and this can be realized by reducing T_D. However, due to the fact that T_D cannot be negative, the best applicable V_{ref} is 0.28 V to achieve the lowest t_{bd}.

In Figure 15, the P_{COND} and P_{BD} losses are minimum at V_{ref} = 0.27 V. Here, when V_{ref} is less than 0.27 V or greater than 0.3 V, these losses will increase. It is also seen in the figure that the MOSFET's conduction loss is slightly higher at V_{ref} = 0.3 V due to the presence of T_D = 15 ns. The role of the controller is to minimize the T_D for the lowest possible P_{COND} by detecting it before S_2 can be turned on. However, this is valid only if T_D is positive. The t_{bd} is slightly higher at V_{ref} = 0.27 V compared to 0.3 V because the high possibility of cross-conduction.

The next study looks at the application of PGD control scheme to the Q_4-switch (PGD-Q_4) of the proposed dual-channel RGD circuit. The process in determining the SRBC switching losses is similar to the PGD-S_2 implementation. Table VII gives the comparative assessments between PGD-Q_4 and PGD-S_2 for V_{ref} = 0.27 V and T_D = 0 ns.

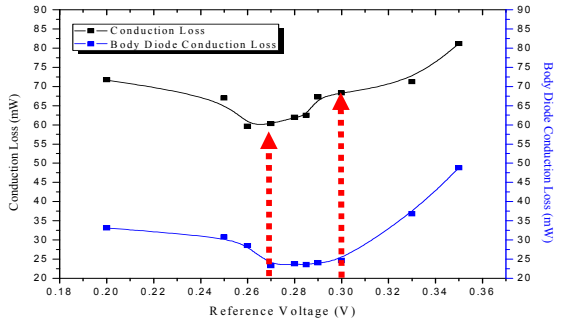

Fig. 15. Relationship between P_{COND} and P_{BD} Vs V_{ref}

TABLE VII. COMPARISON OF PGD-Q_4 AND PGD-S_2 FOR V_{ref} = 0.27 V, D = 20 % AND T_D = 0 ns

Parameters Analyzed	PGD-Q_4	PGD-S_2	% Δ
V_o (V)	10.20	10.02	1.76
I_{Lo} (A)	1.56	1.58	1.27
t_{bd} (ns)	26	27	3.70
P_{COND} (mW)	62.30	60.25	3.29
P_{BD} (mW)	23.65	23.20	1.90
$P_{sw,S1}$ (W)	1.25	1.20	4.00
$P_{sw,S2}$ (W)	1.18	1.15	2.54
$P_{sw,Total}$ (W)	2.52	2.43	3.57

Table VII reveals the impact on utilizing the RGD network with PGD control block. The P_{COND} is seen slightly higher in PGD-Q_4 scheme of 62.30 mW which gives a reduction in 3.29 % compared to PGD-S_2. Also, since the T_D is assumed to be zero at V_{ref} = 0.27 V, ideally, P_{BD} can be minimized. However, this will slightly increase t_{bd} compared to V_{ref} at 0.3 V and hence shoots up S_1 switching loss. In spite of this drawback, the PGD controller is still able to control and adjust S_2 gate signal and maintain P_{COND} and P_{BD} losses at low levels.

By introducing a small interval of 15 ns T_D as given in Table VIII, the issue in signal overlapping can be avoided. In fact, the PGD controller can have a longer safe time margin to detect the T_D before $V_{gs,S2}$ can be turned on. The application of non-zero T_D may in turn give rise to higher P_{COND} and P_{BD}. Remarkably, S_1 switching loss is reduced compared to V_{ref} at 0.27 V leading to lower total switching loss for a shorter duration in t_{bd}.

TABLE VIII. COMPARISON OF FDR AND PGD-S_2 AT V_{ref} = 0.3 V FOR D = 20 % AND T_D = 15 ns

Parameters Analyzed	FDR	PGD-S_2	% Δ
V_o (V)	10.18	10.24	0.59
I_{Lo} (A)	1.51	1.52	0.65
t_{bd} *(ns)*	24	24	-
P_{COND} (mW)	68.30	68.27	0.04
P_{BD} (mW)	25.73	24.60	4.39
$P_{sw,S1}$ (W)	1.14	1.16	1.72
$P_{sw,S2}$ (W)	1.10	1.10	-
$P_{sw,Total}$ (W)	2.33	2.35	0.85

In addition, the use of the proposed dual-channel RGD (FDR) circuit can also be considered as an independent gate drive control option to bias S_1 and S_2 gates. The total switching loss in FDR is only 0.85 % lower than PGD-S_2. However, PWM signals have to be generated with precise control to avoid cross conduction even though it is known for its simplicity. From the evaluation, PGD-S_2 is found to be the best option for the gate drive control mechanism. Apparently all simulation results have indicated positive remarks and brought to successful analyses in the comparison of different PGD driving techniques with the FDR scheme.

C. *Efficiency Comparison*

The efficiency is measured based on the proposed SRBC circuit with fixed load and input values. The gate drive control schemes: AGD and PGD are applied to Q_4 and S_2 respectively in each case. It is observed in Figure 16 that the use of PGD control scheme gives a higher efficiency of more than 82 % at I_{Lo} of 1.5 A compared to AGD and FDR. In addition, the application of AGD-Q_4 produces better efficiency compared to AGD-S_2 by only 2 % because RGD helps control $V_{gs,Q4}$ turn-on for the generation of S_2 pulses. This indicates the necessity of having gate drive circuit in SRBC. However, PGD control scheme does not require any intermediate RGD circuit to achieve high efficiency. The application of PGD-S_2 can reduce the switching loss effectively as S_2 gate can intelligently be adjusted and controlled with respect to the detection of T_D in the circuit.

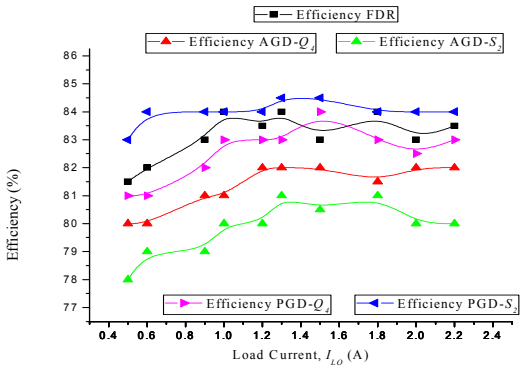

Fig. 16. Efficiency of Gate Drive Control Schemes Vs I_{Lo} for D_{S1} = 20 %, D_{S2} = 75 % and T_D = 15 ns on Proposed SRBC Circuit

In FDR scheme, the driving pulses given to Q_1-Q_4 switches can be precisely controlled by independent PWM generators. It is found that FDR scheme can also manage to cap the efficiency high of 83 % which is comparable to PGD-S_2 implementation. Due to its simplicity, it can be considered since the complemented signals generated at the gates of S_1 and S_2 are easy to control and monitor in accordance with any design requirements.

CONCLUSION

As PGD scheme is concerned, the total switching loss has improved slightly by 1 % compared to the FDR scheme which indicates the feasibility of the design. However, PGD is not easy to be implemented. It has been proven in the work that FDR can manage to sustain a low value of body diode conduction time even though there is a risk in shoot-through current due to its simplicity in design. The AGD and PGD schemes are beneficial to improve the gate driving loss but the design is complex. Comparatively, FDR scheme is easy to apply and eventually gives better advantages in converter's performance. Therefore, the stand-alone FDR control or a direct implementation of PGD-S_2 scheme can be chosen as an easy alternative in the design of high frequency SRBC circuit.

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