A Parallel-SSHI Piezoelectric Energy Harvesting Interface with Efficient Maximum Power Point Tracking Using Half-Cycle Sampling Technique

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ABSTRACT

Efficient Maximum Power Point Tracking (MPPT) in vibration energy harvesting systems commonly relies on the Fractional Open Circuit Voltage (FOCV) technique, which requires fast and accurate sampling of the Open Circuit Voltage (VOC). However, conventional FOCV approaches that periodically open the Rectifier (REC) output suffer from long VOC settling times, leading to increased power losses and degraded tracking efficiency. This paper presents a fast half-cycle VOC sampling technique and its application to a Parallel Synchronized Switch Harvesting on Inductor (P-SSHI) rectifier-based interface circuit. By opening the piezoelectric energy harvester via the negative-voltage converter rather than the REC output, the proposed method enables VOC sampling in only half of the vibration cycle while minimizing the MPPT phase. In addition, operation-aware block enabling is employed to further reduce circuit power consumption. The proposed interface circuit was designed in a 0.35-μm CMOS process. Simulation results demonstrate that the circuit delivers 19.5-89.0 μW to the load over an input range of 0.75-1.6 V at 150 Hz. The achieved MPPT efficiency exceeds 97.7%, peaking at 98.6%, while the Power Conversion Efficiency (PCE) exceeds 96.1%, peaking at 97.4%. The proposed approach significantly reduces MPPT-induced power loss and is well-suited for low-power vibration energy harvesting applications.

Keywords-energy harvesting; piezoelectric; maximum power point tracking (MPPT); FOCV; P-SSHI rectifier

I. INTRODUCTION

Energy harvesting-based power supplies have been studied for various applications requiring long-term and maintenance-free operation [1]. Wireless Sensor Networks (WSNs) are representative applications of such systems, in which energy harvesting techniques can significantly extend system lifetime and eliminate the need for battery replacement [2]. Various interface circuits and energy-harvesting techniques have been proposed to efficiently extract energy from ambient sources and to manage the harvested energy [3,4]. All energy transducers deliver the maximum available power at the Maximum Power Point (MPP). Since the MPP varies with environmental conditions, the application of Maximum Power Point Tracking (MPPT) techniques is required.

Piezoelectric Energy Harvesters (PEHs), widely used in vibration energy harvesting systems, generate AC waveforms; therefore, a Rectifier (REC) is required to convert the output to DC. Various types of PEH rectifiers have been developed and applied to vibration energy harvesting systems, including Full Bridge Rectifiers (FBRs) [4-6], Synchronized Switch Harvesting on Inductor (SSHI) rectifiers [7-10], and Synchronized Switch Harvesting on Capacitor (SSHC) rectifiers [11-14].

The Fractional Open Circuit Voltage (FOCV) method is widely employed for MPPT in vibration energy harvesting systems because it can be implemented simply with relatively low cost. In the FOCV method, the REC output is periodically opened, and the VOC is sampled to determine the MPP Voltage (VMPP). For efficient operation, it is necessary to minimize the REC output open duration, referred to as the MPP Tracking Phase (MTP), while maximizing the Energy Harvesting Phase (EHP).

In SSHI rectifiers, the VOC level is typically high, resulting in a long settling time to reach the VOC. Moreover, voltage limitations during fabrication make the direct application of the FOCV method challenging. Therefore, in [11], an MPPT circuit based on the hill-climbing method was implemented instead of the FOCV approach. However, this method requires complex power-sensing circuitry and suffers from high current consumption. SSHC rectifiers employing new FOCV techniques to reduce VOC sensing time have been proposed [12-14]. Instead of opening the REC output, these approaches

open the PEH output to sense the FBR Open-Circuit Voltage (VOC, FBR) and determine VMPP accordingly. Using this VOC, FBR-based FOCV technique shortened the VOC sensing times to 1.5 cycles [12, 13] or 1 cycle [14].

This paper proposes a Parallel Synchronized Switch Harvesting on Inductor (P-SSHI) REC that adopts the VOC, FBR-based FOCV technique to achieve a fast VOC sensing time of 0.5 cycles. By opening the PEH using a clock synchronized with the vibration, the PEH output reaches VOC within approximately half a cycle. Immediately after VOC sampling, the system transitions to the EHP, thereby minimizing the MTP interval. As a result, MTP is significantly reduced, improving the overall system efficiency. In addition, each functional block is enabled only during its required operation interval, minimizing the circuit power consumption.

II. PROPOSED MPPT INTERFACE CIRCUIT

A. Overall Circuit Architecture

The simplified architecture of the proposed MPPT interface circuit for vibration energy harvesting is shown in Figure 1. The energy generated by the PEH is delivered through the P-SSHI REC and stored in CREC (10 μF). Bias Flipping (BF) operation is periodically performed by connecting the inductor LBF (56 μH) in parallel with the PEH through the control signals VGP and VGN generated by the Flipping-Time Controller (FTC). The FTC operates in synchronization with VAD, which is the output of the Active Diode Comparator (CPAD). The bias generator is implemented using a beta-multiplier structure and provides the Reference Current (IREF) and Reference Voltage (VREF) to the functional blocks. When the REC output voltage VREC is boosted to a level sufficient for MPPT operation (approximately 1.5 V), the voltage detector composed of a resistive divider and a hysteresis comparator generates the ENmt signal, thereby activating the MPPT Controller (MTC).

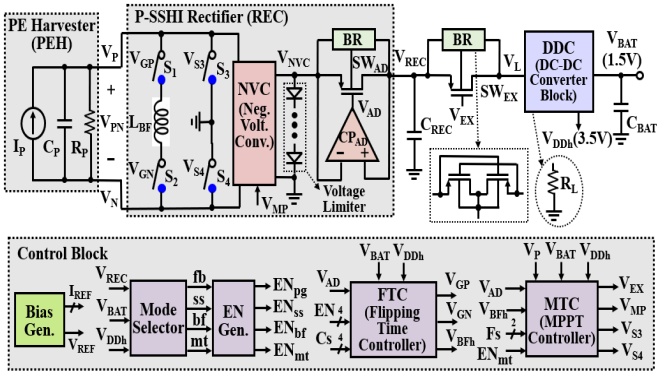

Fig. 1. Simplified block diagram of the proposed MPPT interface circuit.

As displayed in Figure 2, the MTC generates the MPPT Pulse (VMP) to open the PEH every N vibration cycles. During VMP, the internal switches of the Negative Voltage Converter (NVC) are turned off, as illustrated in Figure 3, thereby disconnecting the PEH from the interface circuit. At this moment, VOC sampling and VMPP generation are performed. The MTC compares VREC with VMPP and generates the control signal VEX to determine the on/off state of SWEX, maintaining VREC near VMPP. When SWEX is shorted, the DC-DC Converter (DDC) block operates to charge CBAT (VBAT=1.5 V). In addition, the DDC generates the high voltage VDDh (3.5 V) required for FTC operation [7]. To prevent the body diode of the PMOS switch in the NVC from turning on, the High-Voltage (HV) selector, illustrated in Figure 3, applies the higher of VDDh and VNVC to the body terminal. The AD Comparator (CPAD), which detects the zero crossing of the PEH current source IP, is implemented using a Common Gate (CG) structure, as shown in Figure 4.

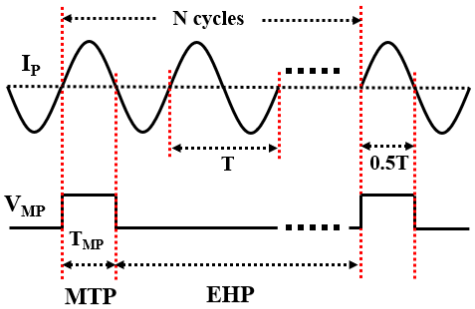

Fig. 2. Timing diagram of the MPPT pulse.

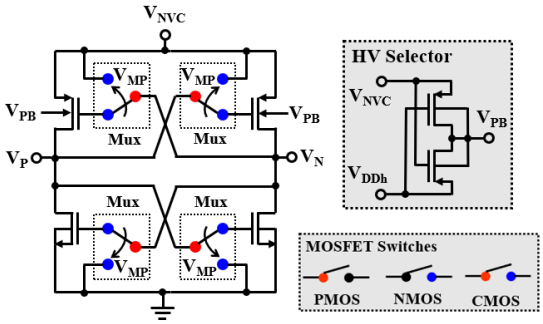

Fig. 3. NVC HV selector and switch symbols.

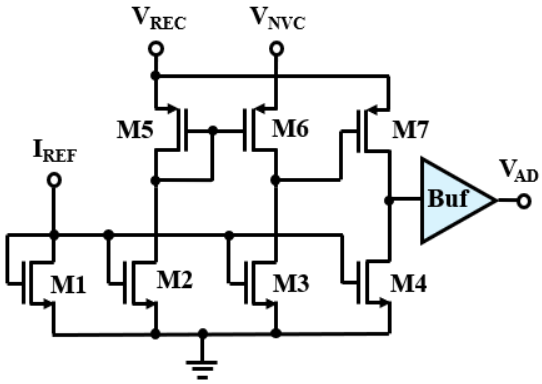

Fig. 4. CPAD.

For higher system efficiency, the MTP should be as short as possible relative to the EHP, thereby reducing the duty cycle of VMP. A lower MPPT frequency (fMP), that is, a larger N, reduces the Power Loss Rate (PLR). However, if fMP is too low in environments where the MPP varies frequently, MPPT cannot be performed promptly, which may increase the PLR. Therefore, in this work, a 2-bit control signal FS is used to select fMP from 1/16, 1/32, 1/64, and 1/128 based on the operating environment. A voltage limiter composed of PMOS diodes is connected to the NVC output to ensure that VNVC does not exceed the process voltage limit. In this work, the interface circuit excluding the DDC block was designed, and during verification, the DDC block was replaced with a load resistor RL.

The proposed circuit supports four operating modes: full-bridge (fb) mode, synchronized-switch (ss) mode, bias-flip (bf) mode, and MPPT (mt) mode. The fb mode is used when VBAT is too low to operate the control blocks. In this case, the REC operates in fb mode to charge CREC and subsequently charge VBAT through the DDC. The ss mode is used when sampling VMPP and can also operate independently. The bf mode is typically used together with the mt mode to perform MPPT. When the bf mode operates alone, the VOC is typically large (6 V in this case), and the peak voltage is limited to 3.8 V by the voltage limiter, as exhibited in Figure 5.

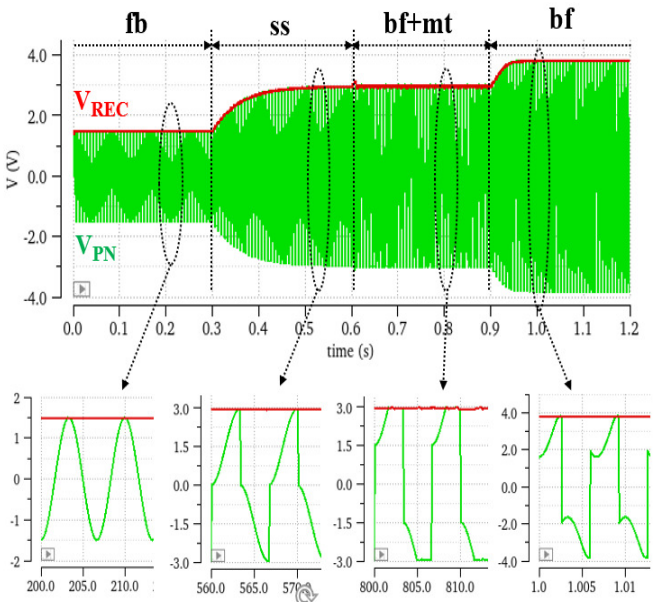

Fig. 5. Waveform characteristics for different operating modes.

B. MPPT Technique of the Proposed P-SSHI REC

The analytical formulation of the P-SSHI REC is described in detail in [7]. The output power of the REC is given by (1), and the maximum output power is obtained in (3) when V_{REC} equals the V_{MPP} defined in (4). The quality factor Q_{BF} in (5), which represents the parallel combination of the PEH quality factor (Q_P) and the L_{BF} quality factor, can be approximated by (7) when Q_P is relatively large.

$$P_{REC} = 2f_P C_P V_{REC}\left(2V_{OC,FBR} - \frac{V_{REC}}{Q_{BF}}\right) \quad (1)$$

$$V_{OC,FBR} = \frac{I_P}{\omega_P C_P} \quad (2)$$

$$P_{REC,max} = 2f_P C_P V_{OC,FBR}^2 Q_{BF} \quad (3)$$

$$V_{MPP} = V_{OC,FBR} Q_{BF} \quad (4)$$

$$Q_{BF} = \left(1 - e^{-\tau} + \frac{\pi k_{BF}}{Q_P}\right)^{-1} \quad (5)$$

$$Q_P = \omega_P C_P R_P, \quad \tau = \pi\left(\frac{4L_{BF}}{C_P R_{BF}^2} - 1\right)^{-1/2} \quad (6)$$

$$Q_{BF} \approx (1 - e^{-\tau})^{-1} = \frac{1}{2}(1 - \eta_F)^{-1} \quad (7)$$

In this design, Q_{BF} was set to approximately 2, considering the process voltage limitations, and the associated component values are: C_P = 60 nF, R_P = 5 MΩ, L_{BF} = 56 µH, and R_{BF} = 12.8 Ω. Under these conditions, the Flipping Efficiency (η_F) is approximately 0.75, as can be verified from (7). It is necessary to maintain R_{BF}, defined as the sum of the parasitic resistance of L_{BF} and the on-resistance of the switches, at a constant value. To achieve this, the technique proposed in [7] was adopted to keep the gate overdrive voltages of the switches (S_1, S_2) constant during the BF operation.

C. Proposed Fast Sampling Technique

To perform FOCV-based MPPT, sampling of the REC VOC is required. A conventional approach widely used in prior work samples VOC at the REC output (V_{REC}) [6], [10]. However, due to the relatively large capacitor connected at the REC output, the time required to reach VOC after opening is long (2 cycles [6], 32 cycles [10]), thereby increasing the PLR. A second approach samples at the PEH output terminals (V_P, V_N) [14, 15]. This method enables faster sampling of the VOC ($V_{OC,FBR}$) (approximately 1.5 cycles), but the additional switches degrade overall power efficiency. In this work, as displayed in Figure 3, the PEH is opened by turning off the switches in the NVC. This approach disconnects the PEH without introducing additional switches in the current path.

The proposed fast sampling technique operates as follows, and its behavior is illustrated in Figure 6. A pulse V_{BF} for BF operation is generated at every zero crossing of I_P and is converted into the V_{GP} and V_{GN} signals to drive switches S_1 and S_2, as presented in Figure 1. As shown in Figure 6(a), during the V_{MP} pulse interval, V_{GP} and V_{GN} are not generated. Instead, the V_{S3} signal (= V_{BF}×V_{MP}) can be used to turn on S_3 and S_4 to reset CP. In this case, the VOC becomes twice the $V_{OC,FBR}$. If S_3 and S_4 are connected to ground only during the short V_{BF} pulse, VN drifts during the remainder of the VMP interval, causing the final VP value to deviate from $2V_{OC,FBR}$, and resulting in inaccurate V_{MPP} sampling. In the proposed design, V_{S4} (= V_{BF}+V_{MP}) is applied to S_4 instead of V_{S3} so that V_N remains grounded throughout the V_{MP} interval. This ensures that the final value of V_P becomes $2V_{OC,FBR}$. Consequently, as demonstrated in Figure 6(b), an accurate V_{MPP} value can be sampled within only 0.5 cycles.

(a)

(b)

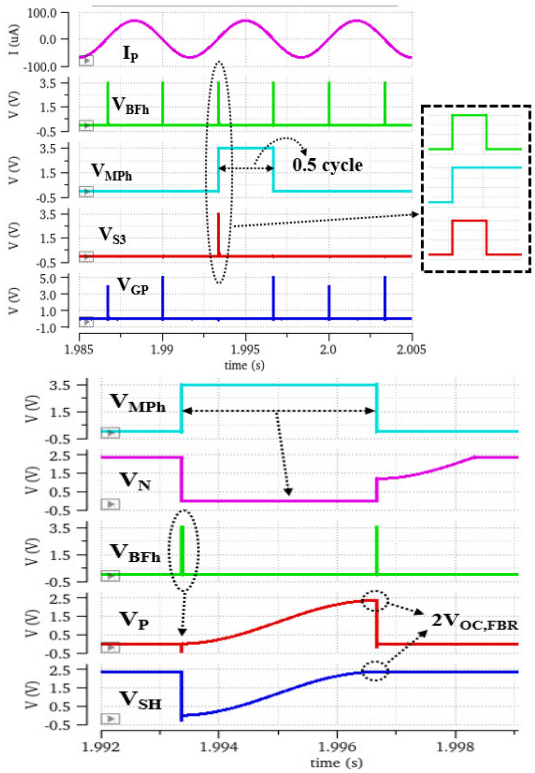

Fig. 6. Operational characteristics of the proposed sampling technique.

D. Flipping-Time Controller

Figure 7 shows the block diagram of the FTC, which consists of a Flipping Pulse Generator (FPG) and a flipping time control circuit. When a rising edge of V_{AD} is detected by the AD, the FPG generates VBF by charging and discharging a small capacitor C_{PG} using the comparator C_{PPG} and associated switches. To adjust the pulse width of V_{BF} to the desired value, a 4-bit control signal C_S is used to tune C_{PG}. As exhibited in Figure 8, the pulse width of VBF is 5.89 µs, and the inductor current ILBF becomes nearly zero at the end of the pulse. After passing through the level shifter, V_{BFh}, with its high level translated to V_{DDh}, is converted into two non-overlapping signals, P_1 and P_2, which are applied to the Switched Capacitor (SC) boost circuit. The SC boost circuit, composed of switches and capacitors, maintains a constant gate overdrive voltage ($V_{G,OD}$) for the BF switches (S_1 and S_2). As shown in Figure 8, during the V_{BF} pulse, the $V_{G,OD}$ values of S_1 and S_2 are held nearly constant at 2.65 V and 2.66 V, respectively.

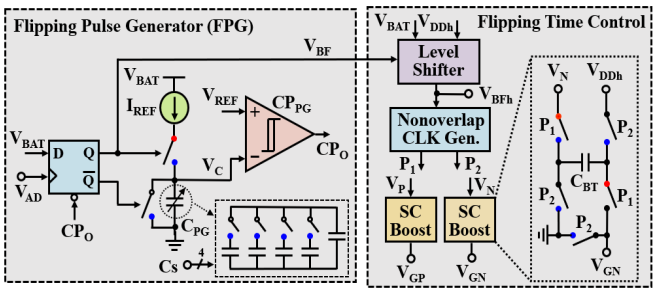

Fig. 7. FTC.

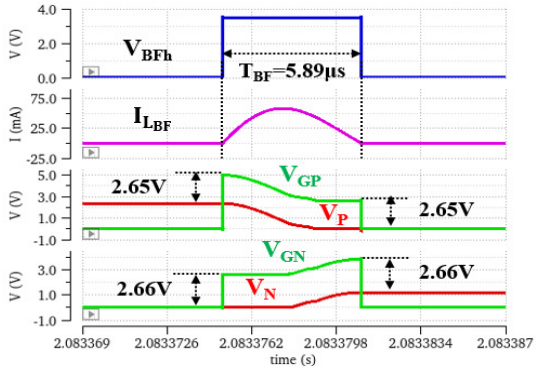

Fig. 8. Simulated waveforms of the FTC.

E. MPPT Controller

Figure 9 illustrates the architecture of the designed MTC, which consists of an MP Generator (MPG), a Peak Detector (PD), and a Sample-and-Hold (S/H) circuit. Figure 10 presents the simulated waveforms for f_P = 150 Hz and I_P = 67.8 µA (V_{MPP} ≈ 2.4 V). In the M_{PG}, the clock signal CK is generated using V_{AD}, and the counter produces the V_{MP} pulse at the division ratio determined by FS. When the peak of V_P is detected by the PD, the D flip-flop is reset, causing V_{MP} to transition low, indicating the completion of the MTP, as shown in Figure 10. The PD consists of a differentiator formed by an Operational Transconductance Amplifier (OTA), CPD, and RPD, followed by the comparator C_{PPD}. When V_P reaches its peak, the PD generates a short-duration pulse V_{PD}. To minimize power consumption, the OTA and CP_{PD} are activated only during V_{MP}.

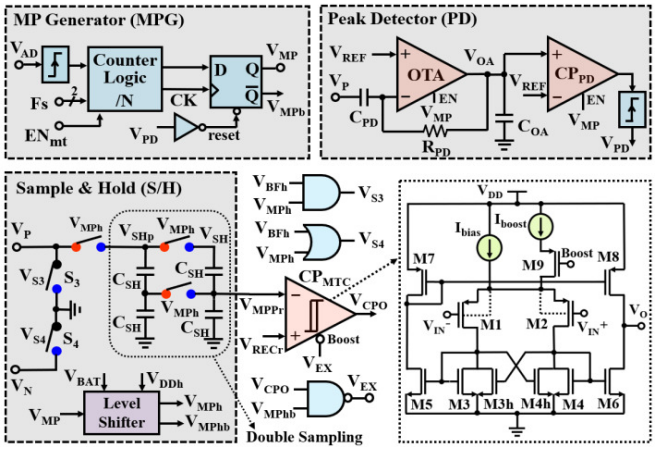

Fig. 9. MTC.

In the S/H circuit, VN is connected to ground during V_{MP}, and V_P is grounded during VBF to reset the PEH capacitor C_P at the beginning of V_{MP}. As a result, the peak value of V_P becomes twice that of $V_{OC,FBR}$, which corresponds to V_{MPP}. The voltage V_{SH} across the two series-connected sampling capacitors C_{SH} (40 pF) tracks V_P during V_{MP}. When V_{MP} falls below a threshold, the peak VP value is sampled, and V_{MPPr} (= V_{MPP}/2) is updated. To reduce VSH variations caused by leakage current, a double-sampling technique is employed in

this design. Because the voltage difference between VSH and V_{SHp} is small when V_{MP} transitions low, the leakage current is reduced. The hysteresis comparator CP_{MTC} compares V_{MPPr} with V_{RECr} (= V_{REC}/2) and generates V_{EX} to control the on/off state of SW_{EX}.

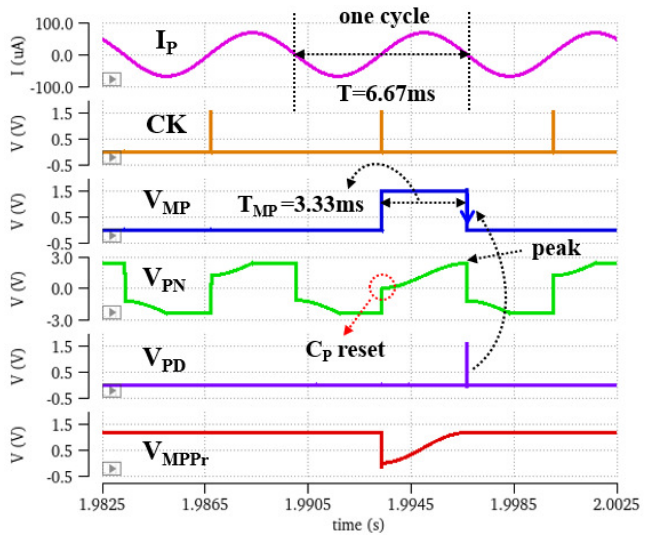

Fig. 10. Simulated waveforms of the MTC.

III. RESULTS AND DISCUSSION

The proposed circuit was designed using a 0.35-μm CMOS process. Figure 11 displays the simulation results under the conditions of I_P = 67.8 μA, f_P = 150 Hz, and f_{MP} = 1/64, and R_L = 10 kΩ. After approximately 0.7 s of start-up time following the onset of vibration and PEH operation, the mode selector generates the mt signal, and the MTC begins operation via the EN_{mt} signal. The V_{MP} pulse is generated every 64 cycles to update V_{MPP}, and V_{REC} is bang-bang controlled within a 34-mV voltage window determined by the hysteresis of comparator CP_{MTC} around V_{MPP}. It can also be observed that the Energy Extraction Phase (EXP), during which power is delivered to the load, occurs in synchronization with this operation.

Figure 12 presents the simulation results to verify the MPPT performance of the designed circuit under varying vibration conditions. In Figure 12(a), the amplitude of IP is fixed at 56.5 μA, while the vibration frequency f_P increases from 100 Hz to 150 Hz and 200 Hz, and then decreases to 120 Hz. Figure 12(b) demonstrates the case where both the amplitude of I_P and f_P vary simultaneously. The values indicated in red brackets on the V_{REC} waveform represent the theoretical VMPP values for each condition. In both cases, the designed circuit accurately tracks the theoretical VMPP values.

When the vibration condition changes, V_{MPPr} is updated in the immediately following MTP, and VREC transitions to the new VMPP. In Figure 12(b), the tracking times required for V_{REC} to reach the new MPP after the vibration change, denoted as T_{tk1} and T_{tk2}, are 0.18 s and 1.39 s, respectively. The tracking time is influenced by several factors, including the vibration conditions (f_P, I_P), f_{MP}, C_{REC}, and R_L. In particular, it varies significantly depending on whether the change in vibration occurs immediately before the MTP (best case) or immediately after it (worst case).

The MPPT efficiency and Power Conversion Efficiency (PCE) of the designed circuit at f_{MP} = 1/64 are shown in Figures 13(a) and 13(b), respectively. The MPPT power efficiency η_P is defined as the ratio of the REC output power P_{REC} to the theoretical maximum power $P_{REC,max}$ in (3). In contrast, the MPPT voltage efficiency η_V is defined as the ratio of the REC output voltage V_{REC} to the theoretical VMPP in (4). The PCE is defined as the ratio of the net output power P_{OUT} of the interface circuit to $P_{REC,max}$. Here, P_{OUT} is calculated by subtracting the power consumed from V_{BAT} and V_{DDh} (P_{BAT} and P_{VDDh}) from the load power P_L delivered by the interface circuit. Within the target input voltage range ($V_{OC,FBR}$ = 0.75-1.6 V), η_P exceeds 97.7%, and η_V exceeds 98.6%, demonstrating that the proposed circuit accurately tracks the ideal MPP. The PCE of the designed circuit is higher than 96.1%, and the output power P_{OUT} ranges from 19.5 to 89.0 Mw.

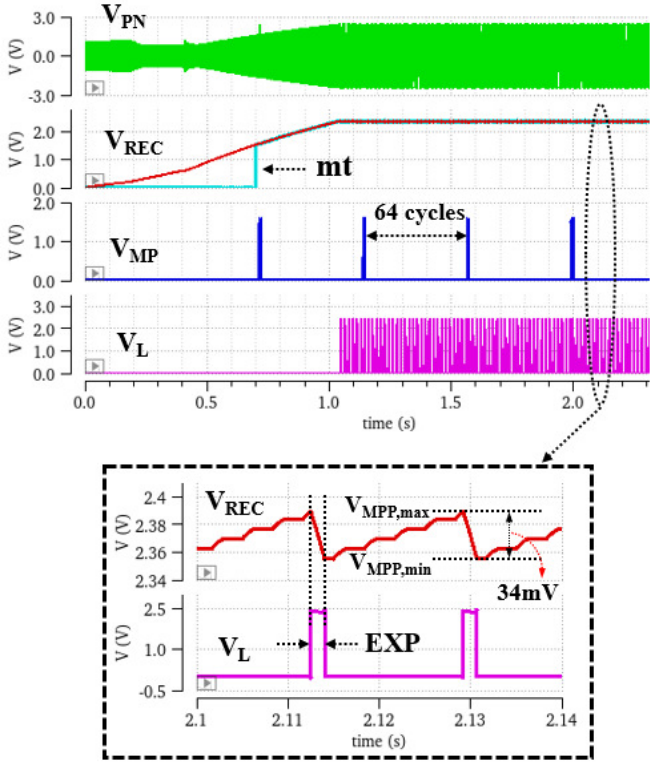

Fig. 11. Overall simulated results of the designed circuit.

Table I summarizes the performance of the designed circuit. Compared with prior circuits employing conventional FOCV techniques, the proposed circuit achieves the shortest VOC sampling time of 0.5 cycles. Accordingly, the PLR is minimized to 0.39% at f_{MP} = 1/128, reducing the additional power overhead required for MPPT. The peak MPPT efficiency and peak PCE reach 98.6% and 97.4%, respectively, demonstrating excellent performance.

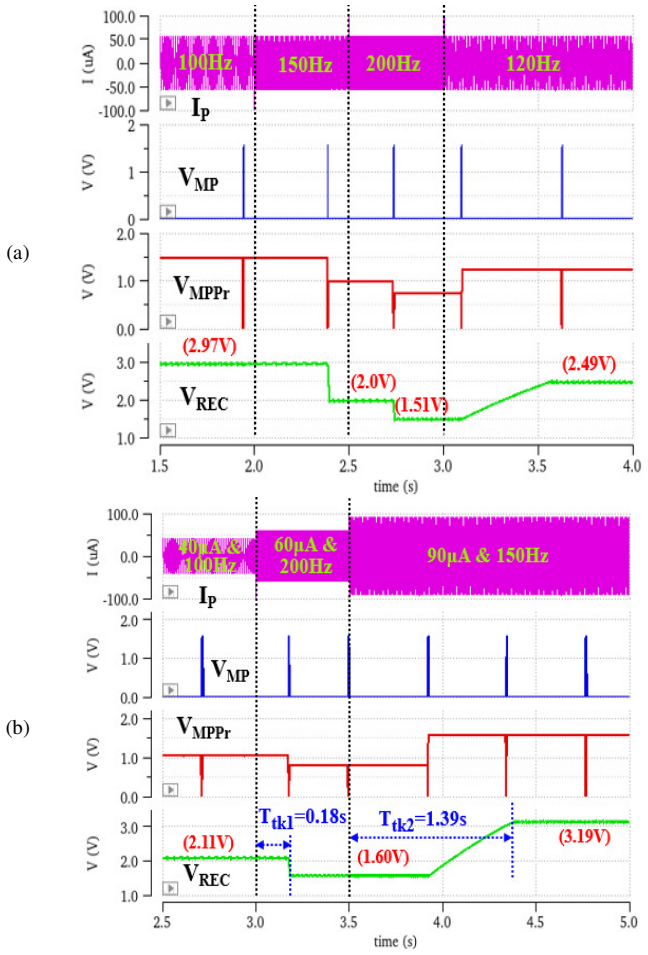

Fig. 12. MPPT characteristics: (a) when f_P varies with I_P fixed at 56.5 μA; (b) when both I_P and f_P vary.

TABLE I. PERFOMANCE COMPARISON

Parameters	This work	[10]	[11]	[13]	[14]
Process (μm)	0.35	0.25	0.13	0.18	0.18
REC scheme	P-SSHI	S-SSHI	P-SSHI	SPFCR	P-SSHC
Input voltage $V_{OC,FBR}$ (V)	0.75-1.6	3-5	2.3-3.9	0.19-1.13	0.98-1.8
Operation frequency (Hz)	150	140	100-180	200	188
MPPT scheme	FOCV	FOCV	P&O	FOCV	FOCV
V_{OC} sampling time (cycles)	0.5	32	N/A	1.5	1.5
PLRa (%)	0.39	25	N/A	1.17	1.17
Flipping efficiency (%)	75.5	N/R	86	84	73.5
Peak MPPT efficiency (%)	98.6	N/R	97	N/R	99.1
Peak power efficiency (%)	97.4	77	78	72	84.3
Output power (μW)	19.5-89	26	100-330	0.5-64	≤ 40

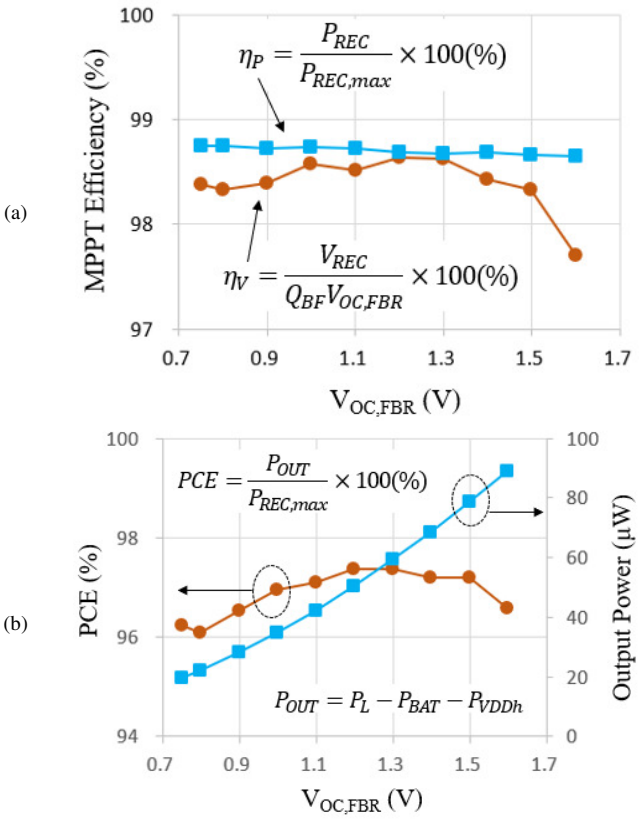

Fig. 13. (a) MPPT power and voltage efficiencies; (b) PCE and output power.

IV. CONCLUSION

This paper presented a fast FOCV-based MPPT interface employing a PEH-side sampling scheme for a P-SSHI rectifier. Unlike conventional FOCV-based approaches that require long V_{OC} sampling times or additional switches at the PEH terminals, the proposed method samples the VOC by disconnecting the PEH via the NVC's internal switches, enabling faster, more efficient operation. By sampling the VOC within half of the vibration cycle, the proposed method significantly reduces the MPPT tracking phase and the associated power loss. Compared with prior techniques, which typically require one or more vibration cycles for VOC sampling, the proposed approach achieves a substantially shorter sampling time, resulting in improved tracking speed and reduced energy loss.

The interface circuit, designed in a 0.35-μm CMOS process, achieves the lowest PLR of 0.39% at f_{MP} = 1/128. It delivers an MPPT efficiency higher than 97.7% and a PCE exceeding 96.1% over an input range of 0.75-1.6 V. The peak MPPT and PCE reach 98.6% and 97.4%, respectively, with an output power ranging from 19.5 to 89.0 μW. Furthermore, the proposed architecture avoids additional series switches in the power path and employs an operation-aware block enabling scheme to minimize control power consumption. Owing to its fast-tracking capability, reduced power overhead, and compact

implementation, the proposed interface is well-suited for low-power vibration energy-harvesting systems and can be effectively applied to self-powered sensor nodes and related applications.

DECLARATION OF COMPETING INTERESTS

The authors declare no competing interests.

ACKNOWLEDGMENT

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DATA AVAILABILITY

The data supporting the findings of this study are available from the corresponding author upon reasonable request.

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