Design and Performance Analysis of a Type-III Compensator for a Buck Converter Using the Frequency Response Method

Fahmizal
Department of Electrical Engineering and Informatics, Vocational College, Universitas Gadjah Mada, Indonesia
fahmizal@ugm.ac.id

Priyo Herlambang
Department of Electrical Engineering and Informatics, Vocational College, Universitas Gadjah Mada, Indonesia
priyo.herlambang@mail.ugm.ac.id

Hari Maghfiroh
Department of Electrical Engineering, Universitas Sebelas Maret, Indonesia
hari.maghfiroh@staff.uns.ac.id (corresponding author)

Miftahul Anwar
Department of Electrical Engineering, Universitas Sebelas Maret, Indonesia
miftahwar@staff.uns.ac.id

Muhammad Hamka Ibrahim
Department of Electrical Engineering, Universitas Sebelas Maret, Indonesia
hamka@staff.uns.ac.id

Joko Slamet Saputro
Department of Electrical Engineering, Universitas Sebelas Maret, Indonesia
jssaputro89@staff.uns.ac.id

Isa Ali Ibrahim
School of Information and Communications Tech, Federal University of Technology, Owerri, Nigeria
ibrahim.ali@futo.edu.ng

Muhammad Ahmad Baballe
Department of Mechatronic Engineering, Nigerian Defence Academy (NDA), Kaduna, Nigeria
mb.ahmad@nda.edu.ng

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ABSTRACT

This study presents the systematic design and performance evaluation of a Type-III compensator for a non-ideal buck converter using a frequency-response-based approach and the K-factor method. The converter is modeled using state-space averaging, incorporating inductor current and capacitor voltage as state variables. Additionally, it accounts for practical non-idealities, such as capacitor ESR and supply-voltage variations. The compensator is designed to achieve the desired phase margin and enhanced closed-loop stability, considering on the open-loop characteristics. The results revealed that compared to a

conventionally tuned Proportional–Integral–Derivative (PID) controller, the proposed Type-III compensator significantly improves transient and steady-state performance. Under constant-load conditions, the settling time decreases from 967.88 µs to 519.23 µs, and the overshoot from 14.11% to 10.11%. Moreover, ripple voltage is suppressed from 181.25 mVpp to 20.84 mVpp, demonstrating improved damping and voltage regulation capability. Under variable-load conditions, the compensator consistently achieves faster recovery and smaller voltage deviation during sudden load changes. Among the evaluated configurations, the 60° phase-margin design provides the best trade-off between transient speed, stability margin, and ripple suppression. Overall, the results confirm that frequency-response-based Type-III compensation constitutes an effective control strategy for non-ideal buck converters, which require high stability and low output-voltage ripple under varying operating conditions.

Keywords-buck converter; frequency response; type-III compensator; PID

I. INTRODUCTION

Electronic circuits operate under varying voltage conditions. To ensure the optimal and safe function of the systems, voltage should be properly regulated. DC-DC converters can be utilized to regulate the input voltage so that the output voltage meets the required specifications [1]. The former utilize semiconductor switches, passive components, and diodes to transfer energy. Non-ideal conditions in a buck converter, caused by component resistances and bias voltages, result in changes to both transient and steady-state performance [2].

The implementation of a control system in a buck converter generates an error signal that serves as a reference for the comparator circuit. This enables the production of a Pulse Width Modulation (PWM) signal for driving the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). Although advanced nonlinear control strategies, such as Fuzzy Logic Control (FLC) and Sliding Mode Control (SMC), have demonstrated improved effectiveness in power converter applications [3], their complex implementation and parameter tuning requirements may limit their practicality in frequency-domain-oriented industrial design environments. Consequently, classical frequency-response-based compensator design is widely adopted in stability-critical applications due to its analytical transparency and systematic tuning procedure [4].

The frequency response method is an analytical method for the dynamic analysis of DC-DC converters, especially in terms of stability and transient response characteristics. This method involves using small signal modeling of the frequency response of the DC-DC converter, which is significant for effective control strategy design. The advantages of the frequency response method include the ability to analyze the stability and bandwidth of a system by analyzing the phase and gain of the transfer function at different input frequencies utilizing a Bode plot. Using the gain margin, phase margin, and crossover frequency of the frequency response parameters of a DC-DC converter, it is possible to determine its stability and transient response characteristics [5].

The frequency response method relies on the placement of poles and zeros in the compensator transfer function. Their locations are used to adjust the gain and phase at specific frequencies so that the desired phase margin and crossover frequency can be achieved. A Type-III compensator is commonly used in DC-DC converters because it can provide up to 180° of phase boost and minimize steady-state error due to the presence of a free pole [6]. Despite the extensive use of buck converters, the systematic design of a Type-III compensator for non-ideal converter conditions using a frequency-response approach remains limited, especially when accounting for parasitic components that significantly influence stability and transient behavior.

Although Type-III compensators are widely employed, there are several limitations. The impact of parasitic elements on loop stability is often neglected, focusing primarily on ideal converter models. In addition, compensator design is often performed for a single target phase margin without systematically investigating how variations the latter influence overshoot, ripple, and load-transient response. Furthermore, comparative benchmarking against classical Proportional–Integral–Derivative (PID) controllers under identical non-ideal plant conditions is not always comprehensively addressed. As a result, practical design insights regarding phase-margin selection and its performance trade-offs are limited.

To address these research gaps, the main contributions of this study are:

1. Development of a non-ideal small-signal model of a buck converter incorporating parasitic elements to reflect realistic operating conditions.
2. Systematic frequency-response-based Type-III compensator design with multi-phase-margin variation analysis.
3. Quantitative comparison between the Type-III compensator and the PID controller under identical non-ideal converter parameters.

II. BUCK CONVERTER

A. Non-Ideal Buck Converter

The non-ideal parameters of a buck converter modify its transfer function through the addition of a zero caused by the capacitor's Equivalent Series Resistance (ESR), which affects both transient and steady-state conditions [7]. Parasitic effects of active and passive components also contribute to a reduction in output voltage [2].

The transfer functions for the buck converter and the compensator were created using the MATLAB simulation tool to obtain the frequency characteristics utilizing the Bode plots, while the LTspice simulation was carried out by employing the non-ideal component values specified in Table I, the circuit diagram depicted in Figure 1, and the switching frequency of 100 kHz.

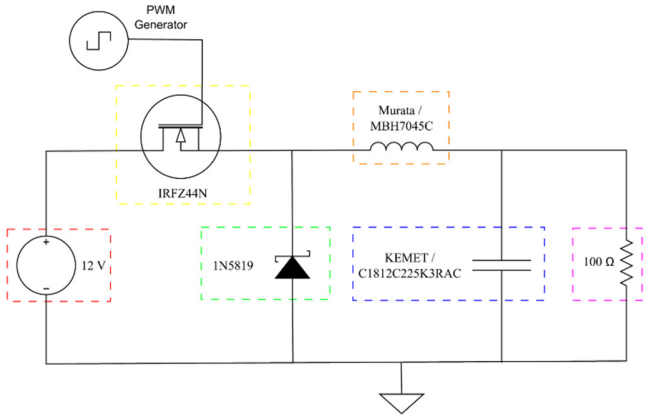

Fig. 1. Buck converter schematic.

TABLE I. BUCK CONVERTER COMPONENTS

Component	Parameter	Value
Battery	Series resistance (R_S)	0.015 Ω
	DC voltage (Vin)	12 V
MOSFET IRFZ44N	On-state resistance (Rdson)	0.0175 Ω
	Threshold voltage (Vth)	3.56 V
Diode 1N5819	Diode resistance (Rdioda)	0.055 Ω
	Forward bias voltage (Vd)	0.34 V
Inductor	Inductor resistance (R_L)	2.28 Ω
	Inductance (L)	1 mH
Capacitor	Capacitor ESR (RC)	0.028 Ω
	Capacitance (C)	2.2 µF
Resistor	Load resistance (Rload)	100 Ω

B. Buck Converter Modeling

A buck converter operates as a nonlinear switching system consisting of two linear subsystems within each switching period: the MOSFET ON (closed) state and the MOSFET OFF (open) state, as described by:

$$\begin{cases}\dot{x}_{on}(t) = A_{on}x(t) + B_{on}u(t)\\ y_{on}(t) = C_{on}x(t) + D_{on}u(t)\end{cases} \quad (1)$$

$$\begin{cases}\dot{x}_{off}(t) = A_{off}x(t) + B_{off}u(t)\\ y_{off}(t) = C_{off}x(t) + D_{off}u(t)\end{cases} \quad (2)$$

To obtain a linear model suitable for compensator design, the standard duty-cycle (D) averaging method is applied. The average state-space matrices are expressed by:

$$\begin{cases}A_{avg} = DA_{on} + (1-D)A_{off}\\ B_{avg} = DB_{on} + (1-D)B_{off}\\ C_{avg} = DC_{on} + (1-D)C_{off}\\ D_{avg} = DD_{on} + (1-D)D_{off}\end{cases} \quad (3)$$

Small-signal perturbations around the DC operating point are defined by:

$$\begin{cases}x = X + \hat{x}\\ d = D + \hat{d}\\ u = U + \hat{u}\\ y = Y + \hat{y}\end{cases} \quad (4)$$

Neglecting second-order perturbation terms $\mathcal{O}(\hat{x}\hat{d})$, the small-signal linear model becomes:

$$\dot{\hat{x}}(t) = A_{avg}\hat{x}(t) + [A_{on} - A_{off}]X\hat{d}(t) + [B_{on} - B_{off}]U\hat{d}(t) \quad (5a)$$

$$\hat{y}(t) = C_{avg}\hat{x}(t) + [C_{on} - C_{off}]X\hat{d}(t) + [D_{on} - D_{off}]U\hat{d}(t) \quad (5b)$$

Applying the Laplace transformation:

$$\hat{x}(s) = (sI - A_{avg})^{-1}\left([A_{on} - A_{off}]X + [B_{on} - B_{off}]U\right)\hat{d}(s) \quad (6)$$

Substituting into the output equation yields the small-signal transfer function from the duty cycle to the output voltage (plant transfer function G_p), expressed by:

$$G_p(s) = \frac{\hat{v}_{out}(s)}{\hat{d}(s)} = C_{avg}(sI - A_{avg})^{-1}([A_{on} - A_{off}]X + [B_{on} - B_{off}]U) + [C_{on} - C_{off}]X + [D_{on} - D_{off}]U \quad (7a)$$

$$G_p(s) = \frac{\hat{v}_{out}(s)}{\hat{d}(s)} = \frac{345.5s + 5.0608*10^9}{s^2 + 6896s + 4.65*10^8} \quad (7b)$$

This transfer function is used in the frequency-response-based compensator design.

III. PROPOSED METHOD

A. Type-III Compensator

A Type-III compensator is a control system used to improve the phase margin and eliminate the steady-state error in a buck converter. This compensator introduces two zeros and three poles, enabling up to 180° of phase boost. One of the poles is placed at the origin to provide integral action for eliminating steady-state error [8]. The general transfer function of the Type-III compensator is given by:

$$G_c(s) = \frac{(1+s/z_1)(1+s/z_2)}{s(1+s/p_1)(1+s/p_2)} \quad (8)$$

To design the compensator, the K-factor method is applied. This method places two zeros at the same corner frequency ω_{zk}, two poles at the same corner frequency ω_{pk}, and one pole at the origin [9]. The transfer function using the K-factor method is expressed by:

$$G_c(s) = K_{\text{dc}}\frac{(1+s/\omega_{zk})^2}{s(1+s/\omega_{pk})^2} \quad (9)$$

The zero and pole corner frequencies are determined based on the desired phase margin at the gain crossover frequency ω_{gcf}. The K-factor is described by:

$$\begin{cases}K_{\text{value}} = \frac{1+\sin(\phi_m - \angle G_p(j\omega_{\text{gcf}}))}{1-\sin(\phi_m - \angle G_p(j\omega_{\text{gcf}}))}\\ \omega_{zk} = \frac{\omega_{\text{gcf}}}{K_{\text{value}}},\ \omega_{pk} = \omega_{\text{gcf}}K_{\text{value}}\end{cases} \quad (10)$$

The parameter K_{value} determines the location of the compensator zeros and poles, while the DC gain K_{dc} is adjusted so that the open-loop transfer function crosses 0 dB at ω_{gcf}. In practical implementation, a Type-III compensator can be realized using an inverting Op-Amp configuration, as displayed in Figure 2.

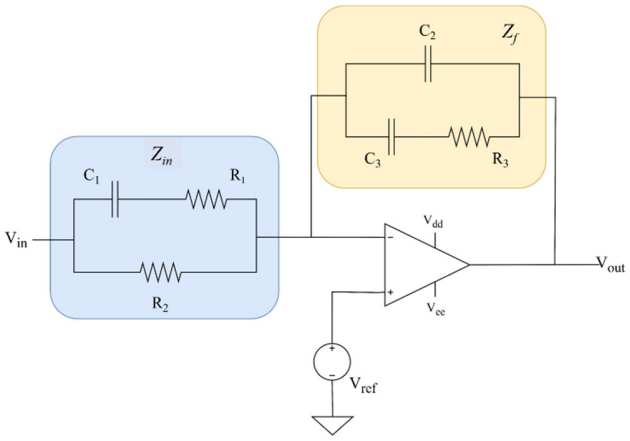

Fig. 2. Type-III compensator control with op-amp.

The transfer function follows the Op-Amp relationship with a negative gain, as expressed by:

$$G_c(s) = -\frac{Z_f(s)}{Z_{in}(s)} \quad (11)$$

where $Z_{in}(s)$is the input impedance network connected to the inverting input of the op-amp, and $Z_f(s)$ is the feedback impedance network connected between the op-amp output and the inverting input. Both networks contain resistor-capacitor combinations that shape the compensator poles and zeros. The passive component values are selected based on K_{value}, ω_{gcf}, and the required compensator magnitude $| G_c(j\omega_{\text{gcf}}) |$. Starting with a chosen R_2, the remaining components are computed by:

$$C_1 = \frac{1}{R_2\omega_{pk}} \quad (12a)$$

$$C_2 = \frac{1}{R_2\omega_{zk}} \quad (12b)$$

$$C_3 = \frac{1}{R_3\omega_{\text{gcf}}} \quad (12c)$$

$$R_1 = \frac{1}{\omega_{zk}C_2} \quad (12d)$$

$$R_3 = \frac{1}{\omega_{pk}C_1} \quad (12e)$$

This compensator adjusts the PWM duty cycle to regulate the output voltage under load or supply variations, thereby improving transient performance and stability.

B. Buck Converter Closed-Loop Design

The K-factor method described in (10) is applied using target phase margins of 45°, 50°, 55°, and 60°. The gain crossover frequency for the frequency-response design is set to 10 kHz. The Type-III compensator is designed based on the closed-loop configuration with negative feedback, as depicted in Figure 3, where the Open-Loop Transfer Function (*OLTF*) consists of the compensator (G_c), plant (G_p), comparator (H_{cmp}), and feedback (H_{fb}) network, as presented in:

$$\text{OLTF}(s) = G_c(s)\, H_{\text{cmp}}(s) G_p(s)\, H_{\text{fb}}(s) \quad (13)$$

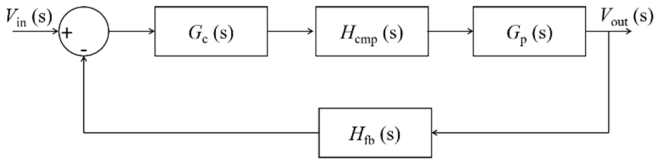

Fig. 3. Closed-loop diagram of the buck converter.

The closed-loop block diagram in Figure 3 yields the Closed-Loop Transfer Function (CLTF), defined by:

$$\text{CLTF}(s) = \frac{G_c(s)\, H_{\text{cmp}}(s) G_p(s)}{1+\text{OLTF}(s)} \quad (14)$$

PWM generation requires a comparator that compares the output of the compensator with a sawtooth waveform of amplitude V_m. In this study, the comparator is modeled as a constant gain, as shown in:

$$H_{\text{cmp}}(s) = \frac{1}{V_m} \quad (15)$$

The feedback gain is also constant:

$$H_{\text{fb}}(s) = \frac{V_{\text{fb}}}{V_{out}} \quad (16)$$

According to (14), the closed-loop system becomes unstable when the denominator $1 + \text{OLTF}(s)$equals zero. This occurs when $\text{OLTF}(s) = -1$; for example, when $|\ \text{OLTF}(j\omega)\ | = 1$ and its phase is $-180°$. Therefore, stability is evaluated using the open-loop transfer function, and the compensator is designed by specifying the gain crossover frequency and the desired phase margin.

The MATLAB-based design procedure for the Type-III compensator is summarized in Algorithm 1. For each target phase margin, the algorithm computes the required K-factor, zero and pole corner frequencies, compensator gain, and Type-III transfer function. The passive component values $R_1, R_2, R_3, C_1, C_2,$ and C_3 are then calculated accordingly and stored for implementation.

Algorithm 1 provides the steps for the Type-III compensator using the K-factor method. The buck converter plant model, desired phase margin, and target crossover frequency are utilized as an input. In the output phase, the design starts with defining the uncompensated plant model for the buck converter, which is followed by specifying the phase margin along with the gain crossover frequency. The phase of the uncompensated plant model is then evaluated at the specified crossover frequency, as well as the phase boost required to achieve the specified phase margin. The K-factor is subsequently determined using the evaluated phase boost, and the compensator poles and zeros are assessed. After that, the Type-III compensator transfer function is determined using the evaluated zeros and poles, followed by the evaluation of the uncompensated open-loop response at the crossover frequency. The compensator gain is then determined to ensure unity gain at the crossover frequency, followed by the implementation of the compensator using passive components. Subsequently, the close-loop response is evaluated to ensure satisfaction of the specified criteria.

The compensator is implemented in the buck converter, as shown in Figure 4. The feedback gain is formed by a voltage divider consisting of 10 kΩ and 5 kΩ resistors, yielding a gain of $\frac{1}{3}$. A unity-gain Op-Amp buffer is used to isolate the divider from the compensator input impedance, preventing interaction between the networks. The complete closed-loop buck converter is implemented and validated using LTspice.

IV. RESULTS AND DISCUSSION

The proposed buck converter with a Type-III compensator controller is validated through simulation using LTspice software. Both constant load and variable load are evaluated. Furthermore, the bandwidth of the closed-loop system is also analyzed.

A. Compensator Type-III Tuning

The constant load used in this test is 100 Ω. Table II shows that the transient-response parameters, rise time, peak time, and settling time, become longer as the phase margin increases. In contrast, a higher phase margin reduces the overshoot, decreasing from 18.45% to 10.11%. The steady-state output voltage remains identical for all compensators at 5.99 V, while the ripple voltage also decreases with larger phase margins, from 28.42 mVpp down to 20.84 mVpp.

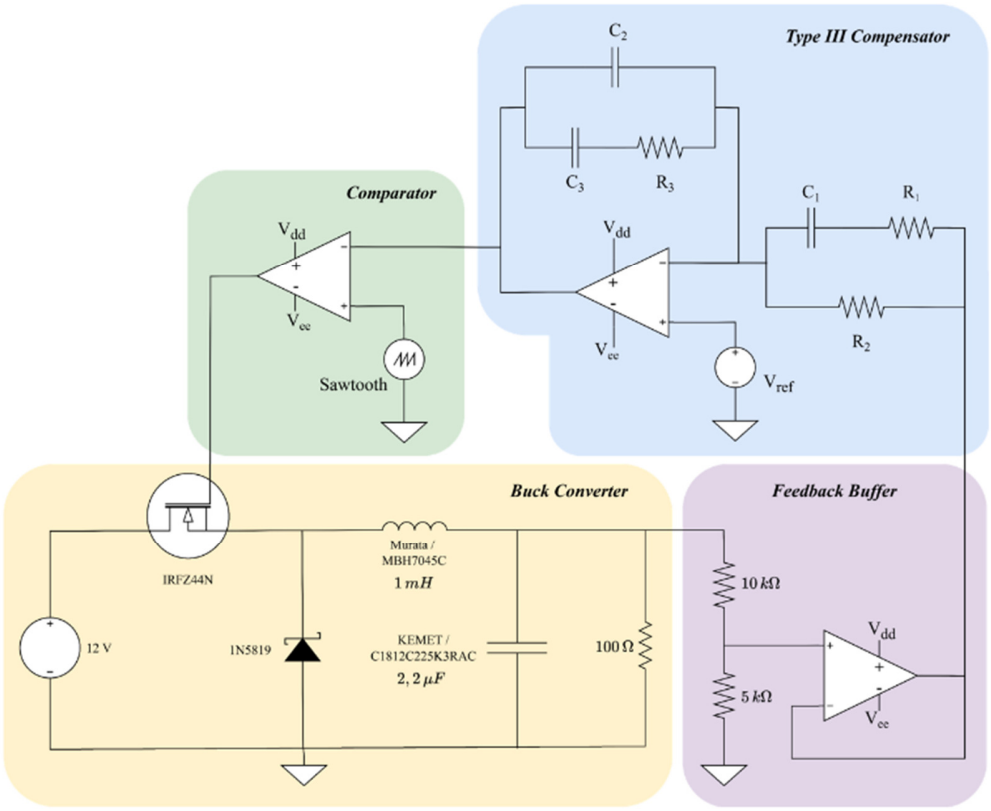

Fig. 4. Completed proposed buck converter with Type-III compensator, comparator, and feedback buffer.

TABLE II. CONSTANT LOAD TESTING RESULTS

Parameter	Phase margin			
	45°	**50°**	**55°**	**60°**
Rise time (µs)	44.54	45.40	48.85	53.09
Peak time (µs)	98.36	126.05	146.16	176.16
Settling time (µs)	410.05	448.50	487.75	519.23
Overshoot (%)	18.45	14.42	12.59	10.11
Steady-state voltage (V)	5.99	5.99	5.99	5.99
Ripple voltage (mVpp)	28.42	26.54	24.11	20.84

The results in Table II demonstrate the relationship between the phase margin and the transient response of the buck converter. With the increase in phase margin, the stability and oscillations of the system improve, as also observed by increasing the rise time, peak time, and settling time. This agrees with the principles of classical control systems, where the phase margin is directly proportional to the damping and the degree of oscillations. However, the increase in phase margin is also directly proportional to the degree of sluggishness in the control system. In the case of the buck converter, the degree of overshoot is highly reduced as the phase margin increases from 18.45% to 10.11% and as the phase angle increases from 45° to 60°. This demonstrates the effectiveness of the Type-III compensator in ensuring that the output voltage is not more than the reference voltage. However, the steady-state output voltage of 5.99 V for all compensators demonstrates the effectiveness of the Type-III compensator in eliminating the steady-state error for a constant load. In addition, the reduction in ripple voltage as the phase margin increases shows the effectiveness of the Type-III compensator.

As presented in Table III, increasing the phase margin results in a more damped response, characterized by slightly reduced voltage deviation and longer settling times. During the transition from 100 Ω to 50 Ω, the compensator with the highest phase margin yields the smallest undershoot, keeping the output voltage closer to its nominal value, while the settling time increases from 47.32 µs to 55.95 µs. A similar trend is observed for the reverse transition (from 50 Ω to 100 Ω), where the overshoot decreases slightly (from 6.36 V to 6.34 V) as the phase margin increases, accompanied by an increase in settling time from 46.38 µs to 59.68 µs.

TABLE III. VARIABLE LOAD TESTING RESULTS

Parameter	45°	50°	55°	60°
Load change: 100 Ω → 50 Ω (load current increase)				
Settling time (µs)	47.32	49.24	52.38	55.95
Undershoot voltage (V)	5.65	5.66	5.66	5.66
Load change: 50 Ω → 100 Ω (load current decrease)				
Settling time (µs)	46.38	47.50	51.55	59.68
Overshoot voltage (V)	6.36	6.35	6.34	6.34

Based on Table III, the performance of the Type-III compensator during step load changes was evaluated for all four phase-margin designs. For the 100 Ω-50 Ω case, the voltage decreases as the phase margin increases, demonstrating improved damping. Although the variation is small, the trend confirms that higher phase margins provide better disturbance rejection. However, this behavior is accompanied by longer settling times, which increase by more than 8 µs across the tested range. For the 50 Ω-100 Ω case, the system exhibits overshoot as it moves toward its new steady-state output. The overshoot steadily decreases with higher phase margins, while the settling time again increases, indicating a similar trade-off between voltage stability and response speed.

The 60° compensator provides the most balanced and desirable performance for this buck-converter application. The results outlined in Tables II and III indicate that increasing the phase margin consistently reduces overshoot, undershoot, and output ripple. Among all tested values, the 60° design achieves the lowest overshoot (10.11%), the lowest ripple voltage (20.84 mVpp), and the lowest overshoot/undershoot during load changes. Although its settling time is longer than the lower-margin designs, the increase remains within an acceptable range and does not impact steady-state accuracy, which remains constant at 5.99 V.

TABLE IV. FINAL TYPE-III COMPENSATOR PARAMETER VALUE

Parameter	Value	Parameter	Value
K_{value}	37.06	R_1 (Ω)	277.30
ω_{zk} (rad/s)	10.32	R_2 (Ω)	10000
ω_{pk} (rad/s)	382.51	R_3 (Ω)	12678
K_{dc} (dB)	82.10	C_1 (nF)	9.428
		C_2 (pF)	211.9
		C_3 (nF)	7.642

The 60° phase margin compensator is chosen as the optimal Type-III configuration because it offers the best voltage stability and damping under varying loads, prioritizing stability over response speed. Its parameters are documented in Table IV for subsequent comparison with a PID controller.

B. Performance Validation

For a fair comparison, the PID controller was designed to achieve the same 60° phase margin as the proposed Type-III compensator. Tuning was performed using MATLAB PID Tuner based on the open-loop transfer function of the non-ideal buck converter. The gain crossover frequency corresponding to the 60° phase margin was 58.80 rad/s, yielding tuned parameters of $K_p = 3.97$, $K_i = 3.6 \times 10^4$, and $K_d = 9.71 \times 10^{-5}$. These parameters were consistently applied in all simulations to ensure an equivalent stability margin.

Figure 5 presents the output voltage response under a constant 100 Ω load. The PID controller exhibits higher overshoot and more pronounced oscillations before reaching a steady state. In contrast, the Type-III compensator produces a smoother transient response with reduced peak deviation and significantly lower ripple.

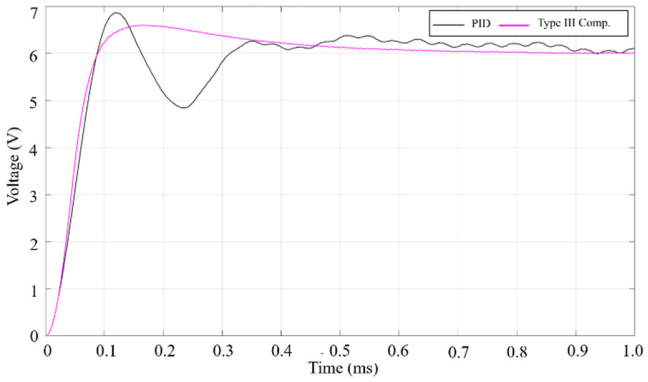

Fig. 5. Constant load of 100 Ω: Type-III compensator versus PID.

According to Table V, the Type-III compensator significantly improves transient performance under constant-load conditions. The settling time is reduced from 967.88 µs (PID) to 519.23 µs, while the overshoot decreases from 14.11% to 10.11%. Although the peak time increases from 120.23 µs to 176.16 µs, the overall convergence to a steady state is substantially faster due to the significantly shorter settling time.

TABLE V. CONSTANT LOAD: COMPARED TO PID

Parameter	PID	Type-III compensator
Rise time (µs)	60.45	53.09
Peak time (µs)	120.23	176.16
Settling time (µs)	967.88	519.23
Overshoot (%)	14.11	10.11
Steady-state voltage (V)	6.00	5.99
Ripple voltage (mVpp)	181.25	20.84

Both controllers achieve nearly identical steady-state output voltages (6.00 V and 5.99 V, respectively). However, the ripple voltage is significantly reduced from 181.25 mVpp to 20.84 mVpp, indicating improved damping and superior voltage regulation performance with the proposed Type-III compensator.

Figure 6 illustrates the output voltage response during a load change from 100 Ω to 50 Ω. The peak voltage deviation is larger in the case of the PID controller, and the oscillatory transient response is more pronounced with a larger settling time and smaller damping factor compared to the Type-III compensator. In contrast, the Type-III compensator yields a shallower voltage dip and smoother stabilization, indicating stronger damping and better robustness to sudden load changes. These observations are consistent with the quantitative results depicted in Table VI.

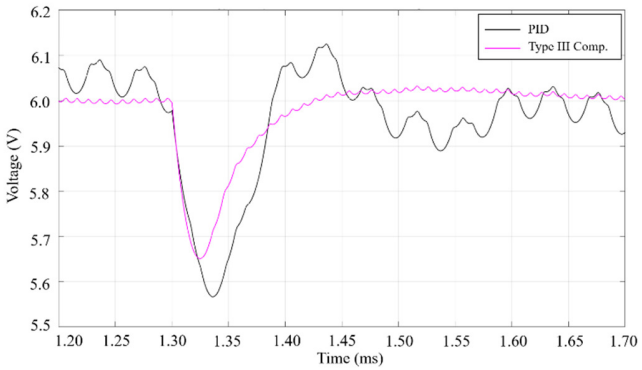

Fig. 6. Load changes from 100 Ω to 50 Ω: Type-III compensator versus PID.

The results in Table VI demonstrate that the Type-III compensator maintains superior transient performance under variable-load conditions.

TABLE VI. VARIABLE LOAD: COMPARED TO PID

Parameter	PID	Type-III compensator
Load change: 100 Ω → 50 Ω (load current increase)		
Settling time (µs)	79.80	55.95
Undershoot voltage (V)	5.57	5.66
Load change: 50 Ω → 100 Ω (load current decrease)		
Settling time (µs)	73.73	59.68
Overshoot voltage (V)	6.46	6.34

During the 100 Ω-50 Ω transition (load current increase), the settling time is reduced from 79.80 µs (PID) to 55.95 µs. In addition, the minimum output voltage improves from 5.57 V to 5.66 V, indicating a smaller voltage deviation from the nominal steady-state value. A similar improvement is observed during the reverse transition, where the settling time decreases from 73.73 µs to 59.68 µs. The overshoot voltage is also reduced from 6.46 V to 6.34 V. These results confirm that the higher phase margin provided by the Type-III compensator enhances damping and reduces voltage deviation during sudden load changes.

V. CONCLUSION

This study presented the systematic design and evaluation of a Type-III compensator for a non-ideal buck converter using a frequency-response-based approach and the K-factor method. The proposed compensator significantly enhances closed-loop performance compared to a conventionally tuned Proportional–Integral–Derivative (PID) controller.

Under constant-load conditions, the Type-III compensator reduces the settling time from 967.88 µs (PID) to 519.23 µs and lowers the overshoot from 14.11% to 10.11%. Moreover, ripple voltage is significantly decreased from 181.25 mVpp to 20.84 mVpp, demonstrating superior damping and improved steady-state voltage quality. Under variable-load conditions, the Type-III compensator consistently achieves faster recovery and smaller voltage deviation during both load-current increase and load-current decrease transitions. For example, during a 100 Ω-50 Ω load change, the settling time improves from 79.80 µs to 55.95 µs, while voltage deviation is reduced. Similar improvements are observed for the reverse transition.

Among the tested configurations, the 60° phase margin provides the most balanced trade-off between transient response, stability, and ripple suppression. Overall, the results confirm that frequency-response-based Type-III compensation offers a robust and highly effective control strategy for non-ideal buck converters, particularly in applications requiring fast dynamic response, high stability margins, and low output-voltage ripple under varying load conditions.

DECLARATION OF COMPETING INTERESTS

All authors declare that they have no conflicts of interest.

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DATA AVAILABILITY

The data used can be made available upon request from the corresponding author.

AI USE AND DECLARATION OF GENERATIVE AI USE

During the preparation of this study, the authors used ChatGPT to improve readability and language. After using this tool, the authors reviewed and edited the content as needed and take full responsibility for the content of the publication.

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