Polymer-Engineered Interfaces for Tailoring Resistive Switching in TiO_2-Based Memristors

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ABSTRACT

Resistive Random-Access Memory (ReRAM) devices constitute a popular Non-Volatile Memory (NVM) solution. Nevertheless, TiO_2-based memristors suffer from instability and low endurance, with the effect of Polymethyl Methacrylate (PMMA) polymer on improving these limitations being unexplored. This study examines the interfacial positioning of PMMA polymeric layers within TiO_2-based memristors. Four device structures were initially fabricated to analyze the effects of PMMA interfacial positioning on several Resistive Switching (RS) parameters using Fluorine-doped Tin Oxide (FTO) and Carbon (C) electrodes: (i) FTO/TiO_2/C, (ii) FTO/TiO_2/PMMA/C, (iii) FTO/PMMA/TiO_2/C, and (iv) FTO/PMMA/TiO_2/PMMA/C. Only FTO/TiO_2/PMMA/C and FTO/PMMA/TiO_2/C demonstrated clear bipolar RS behavior. The FTO/TiO_2/PMMA/C device exhibited the lowest SET/RESET voltage, an ON/OFF ratio of ~10^1, a retention of ~10^4 s, and an endurance of ~10^2 cycles, underscoring the impact of PMMA placement on decreasing the switching threshold. These findings provide a novel strategy for designing next-generation NVM applications, in which the interfacial positioning role of polymers in optimizing ReRAM performance could be effectively understood.

Keywords-resistive random-access memory; PMMA; TiO_2; resistive switching; memristors

I. INTRODUCTION

With the emergence of artificial intelligence and the Internet of Things, great amounts of data are being collected and processed, driving the need for new memory technologies that are affordable, high-speed, and energy-efficient. Such technologies are ReRAM, Phase-Change Memory (PCM), Magnetic Memory (MRAM), and Ferroelectric Memory (FeRAM) [1], all of which fall under NVM, enabling data retention even in the absence of power [2, 3].

ReRAM stands out due to its low cost, low power consumption, high speed, excellent scalability, and compatibility with the Complementary Metal-Oxide-Semiconductor (CMOS) technology [4]. ReRAM devices are also a practical realization of memristors, since they exhibit RS behavior governed by memristive dynamics [5]. Generally, ReRAM is low-cost and highly scalable due to its simple structure (top and bottom electrodes sandwiching an active layer). The most common ReRAM active layers include oxide-based materials (TiO_2), chalcogenide-based materials (GeSe), polymer-based materials (PMMA), graphene-based materials, and perovskite-based materials [6]. Common electrode materials include Al, Pt, C, and Transparent Conductive Oxides (TCOs). Collectively, different types of electrodes and active layers significantly influence the RS characteristics, impacting switching voltage, endurance, retention, and uniformity [5]. The integration of polymers in ReRAM devices has been explored to enhance their performance and reliability. The role of polymers in halide perovskite RS devices improves the ON/OFF ratio, retention, and endurance properties, as they function as passivation layers, charge transfer enhancers, and composite materials. Polymers in metal oxides for ReRAM devices have also been investigated [7]. Authors in [8] reported TiO_2-based memristors, containing poly(4-vinylphenol) (PVP)-molybdenum disulfide (MoS_2) composites [8]. It was revealed that Ag/PVP:MoS_2/TiO_2/Indium Tin Oxide (ITO) possessed low SET and RESET voltages of 1.0 V and -1.2 V, respectively. Both the ohmic conduction and Space Charge Limited Current (SCLC) mechanisms were also confirmed to cause RS behavior in the devices.

PMMA is a strong candidate due to its insulating properties, transparency, flexibility, thermal stability, low cost, and ease of processing [9]. It can be conveniently deposited using solution-based methods (spin coating), making it highly compatible with low-cost fabrication. PMMA exhibits RS behavior. For example, in a perovskite-based structure (Pt/oxide-passivated $MAPbI_3$/PMMA/Ag), the addition of a PMMA layer demonstrated good retention and endurance. Despite these possibilities, the effect of PMMA interfacial positioning in TiO_2-based memristors remains unexplored.

No detailed study has been conducted on the interfacial positioning of PMMA on TiO_2-based memristors, which can significantly influence switching characteristics (defect formation, filament growth, and stability of conduction paths). To fill this research gap, the current study investigated the effect of PMMA interfacial positioning on TiO_2-based memristors to enhance their RS performance.

In this work, four device structures were fabricated to investigate the influence of PMMA on critical parameters. The TiO_2 layer was deposited on the FTO substrates using the spin-coating method, while the PMMA layers were applied via spin-coating in different configurations. Finally, the C electrode was deposited using the doctor blade method with commercial carbon paste.

II. MATERIALS AND METHODS

A. Materials

The TiO_2 used in this study was obtained from Solaronix (Ti-Nanoxide T600/SC). The PMMA powder (molecular weight = 120,000) was purchased from Sigma-Aldrich. Acetone used to dilute PMMA was provided by Emsure®. The C electrode was prepared using C paste obtained from Dycotec (DM-CAP-4701S). All chemicals used in this study were of analytical grade and were utilized as received, meaning without any further purification.

B. TiO_2 and PMMA Solution Preparation

The TiO_2 precursor solution was prepared by diluting 4.2857 mL of a commercial 7 wt% TiO_2 dispersion with 5.7143 mL of absolute ethanol, resulting in a homogeneous solution suitable for spin coating. Meanwhile, the PMMA solution was prepared by weighing the PMMA powder on a weighing dish. This powder was then added to acetone to create a 2.5 mg/mL solution. The mixture was transferred into a vial and sonicated for 10 min to ensure thorough mixing. All these solutions were subsequently sealed and kept in a dry storage area.

C. Polymer-Overlaid TiO_2-Based Memristor Preparation

This study examined the effect of PMMA interfacial positioning on TiO_2-based memristors by varying the PMMA positioning. Thus, four devices were fabricated and constructed on FTO-coated glass substrates measuring 20 × 20 mm, featuring circular top electrodes (diameter = 5.5 mm) (Figure 1): (i) FTO/TiO_2/C (control), (ii) FTO/TiO_2/PMMA/C, (iii) FTO/PMMA/TiO_2/C, and (iv) FTO/PMMA/TiO_2/PMMA/C.

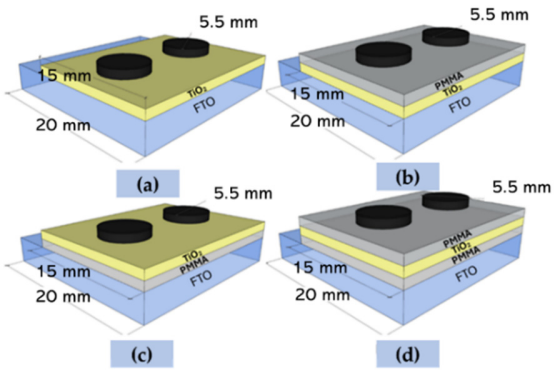

Fig. 1. Schematic structures of the TiO_2-based memristors involving: (a) FTO/TiO_2/C, (b) FTO/TiO_2/PMMA/C, (c) FTO/PMMA/TiO_2/C, and (d) FTO/PMMA/TiO_2/PMMA/C.

All four devices contained three essential layers: (i) TiO_2, (ii) PMMA, and (iii) carbon electrode. Nevertheless, the processing methods for each thin-film type were identical throughout the fabrication process of all four devices. For the TiO_2 layers, the TiO_2 thin films were spin-coated at 3000 rpm for 30 s on either FTO or PMMA. These films were then annealed at 450 °C in a furnace after finishing the layering process. The PMMA thin films were also fabricated on either FTO or TiO_2 at 3000 rpm for 30 s. These films were annealed on a hot plate at 60 °C. Finally, all samples contained carbon-based electrodes utilizing the carbon paste. This final electrode layer was created through the doctor-blade technique, in which the carbon thin film was annealed on a hot plate at 70 °C for 30 min. Overall, all samples were deposited under identical conditions.

D. Characterization Tools

The devices were prepared and characterized using various methods to analyze their electrical and optical properties. The structural characteristics of the thin films were characterized utilizing an X-Ray Diffractometer (XRD, Shimadzu) with Cu Kα radiation (λ = 1.5406 Å) across the 2θ range of 20° to 80°. Field Emission Scanning Electron Microscopy (FESEM, Nova NanoSEM 450) was used to investigate the surface morphology of the prepared films. An Atomic Force Microscope (AFM, Dimension Edge) was utilized for surface roughness calculations. Alternatively, a Fourier Transform Infrared (FTIR) spectrometer (Bruker Invenio R) was employed to examine the chemical compounds. Thickness was measured using a profilometer (MarSurf SD 26), and all samples possessed identical thickness. Finally, Cyclic Voltammetry (CV), Chronoamperometry (CA), endurance, and retention analyses (Autolab PGSTAT204) were deployed to examine the RS behavior of the devices. Each structure contained three duplicates that were repeated three times to obtain the average readings for certain RS parameters. All these analyses were conducted under a compliance current of 10 mA and a voltage sweep rate of 0.1 V/s.

III. RESULTS AND DISCUSSION

A. Structural Characterization of the Fabricated Films

The carbon electrode and TiO_2 thin film were characterized using XRD measurements after annealing at 70 °C and 450 °C, respectively. The XRD pattern of the carbon sample shows a distinct diffraction peak at 2θ of 27.02° (Figure 2(a)). This high peak is characteristic of carbon, confirming the successful fabrication of the carbon top electrode on all four devices. Furthermore, the XRD pattern of the fabricated TiO_2 thin film prepared from the TiO_2 solution exhibited distinct diffraction peaks at 2θ = 25.30°, 46.08°, and 55.23° (Figure 2(b)). These peaks correspond to the characteristic reflections of the TiO_2 anatase phase, aligning well with the standard TiO_2 pattern (JCPDS 00-021-1236) [10]. The successful synthesis of the crystalline anatase TiO_2 structure was validated.

The XRD patterns had been previously collected on ITO substrates due to temporary instrument access constraints. Nevertheless, the identification of anatase TiO_2 was not affected by the choice of TCO substrate, as the TiO_2 peaks were independent of whether FTO or ITO was used [11]. Thus, the peaks observed at 2θ = 30.18°, 35.13°, and 50.13° were attributed to ITO, as identified by the standard ITO pattern (JCPDS 00-039-1058) [12]. These peaks were indicated on the ITO substrates below the formed TiO_2 film. The presence of these peaks is attributed to the extremely thin spin-coated TiO_2 film (approximately 78 nm), a finding was confirmed by the profilometer assessments performed on the TiO_2 films. Collectively, the successful creation of TiO_2 and carbon electrode was effectively demonstrated through this XRD analysis.

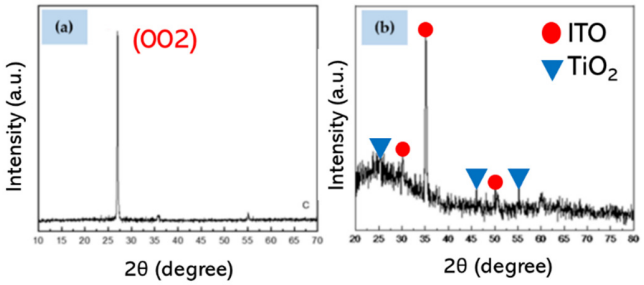

Fig. 2. XRD patterns of: (a) carbon electrode and (b) TiO_2 on ITO.

Figure 3 presents the FESEM images of the carbon-based electrode at magnifications of 50,000× and 100,000×. The images revealed a coral-like structure characterized by a rough, porous morphology. Thus, a high surface area was observed. This porosity was likely attributed to the doctor blade coating technique, which could produce a rougher surface due to the deposition process. Meanwhile, the FESEM images of TiO_2 at different magnifications were examined. These TiO_2 nanoparticles exhibited a uniform size in the nm range (~20-40 nm), and all of them seemed to agglomerate into clusters. However, the interparticle gaps could contribute to a rough and high surface area morphology.

This study proposes that the increased surface area can enhance the contact between the TiO_2 layer and the carbon electrode. Therefore, a higher surface roughness can improve the RS performance by facilitating the formation of larger-diameter conducting filaments [13]. As such, filamentary formation could be accelerated with larger surface roughness.

Figure 4 shows FESEM images of PMMA thin films annealed at 60 °C and 450 °C. The images were obtained at magnifications of 50,000× and 100,000×. The FESEM analysis was conducted to understand the effect of annealing on samples with varying PMMA and TiO_2 layer configurations, as the PMMA layer could degrade at the 450 °C annealing temperature employed for the TiO_2 layer. The degradation can significantly modify the properties of PMMA and the overall RS of the device [9]. Consequently, the PMMA films annealed at 450 °C demonstrated higher surface roughness than the PMMA films annealed at 60 °C. This can be attributed to the increased evaporation of the solvent at higher annealing temperatures. Nonetheless, further confirmation was necessary to ensure that PMMA was still present.

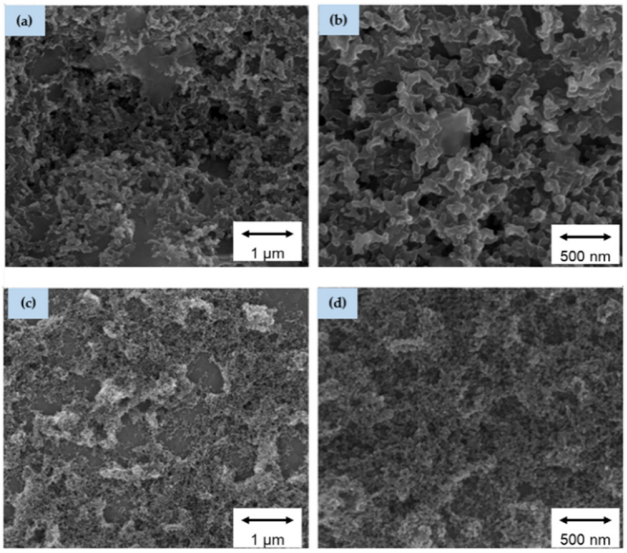

Fig. 3. The FESEM magnifications of carbon at: (a) 50 000× and (b) 100 000×, and TiO_2 at (c) 50 000× and (d) 100 000×.

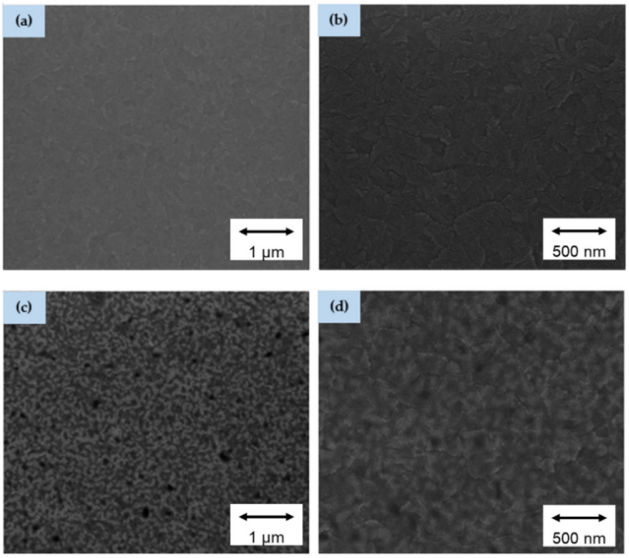

Fig. 4. FESEM images of PMMA films annealed at: 60 °C (a) 50 000× and (b) 100 000×, and at 450 °C (c) 50 000× and (d) 100 000×.

Figure 5 depicts the FTIR spectra for FTO/TiO_2, FTO/TiO_2/PMMA, FTO/PMMA/TiO_2, and FTO/PMMA/TiO_2/PMMA. The FTIR spectra of the annealed films exhibited the distinctive low-frequency metal-oxygen vibrational bands (~400–800 cm^{-1}) characteristic of TiO_2 (Ti–O and Ti–O–Ti) in all samples, confirming the presence of the oxide layer after annealing [14]. All TiO_2-containing samples produced a broad but weak absorption near 3700 cm^{-1} due to the O–H stretching of isolated surface hydroxyl groups (–OH) [15]. A strong absorption around 2350 cm^{-1}, which was present in all spectra, was due to CO_2 of the air [16]. Weak absorptions near ~1730 cm^{-1} and 1140–1260 cm^{-1} were also observed in the FTO/TiO_2 sample, likely due to surface-bound carbonates or residual organics [17].

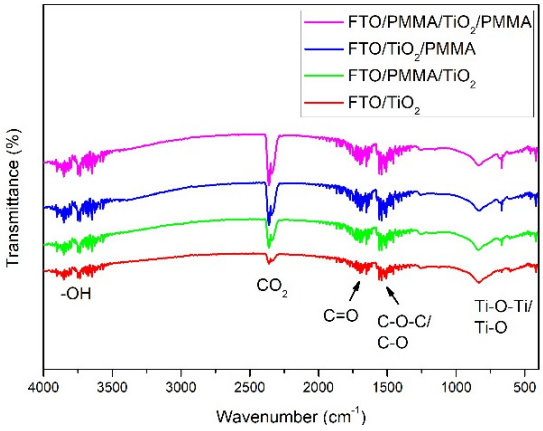

Fig. 5. FTIR spectra.

The PMMA-containing samples revealed C=O stretching vibrations near 1730 cm^{-1}, indicating the presence of ester groups from the PMMA polymer. These samples denoted a series of overlapping peaks in the 1140–1260 cm^{-1} range, which is typical of C–O–C and C–O stretching in the ester backbone of PMMA [18]. This outcome was based on the increased signal intensity in these regions. The C–H stretching region near 2950–3000 cm^{-1} was not observed, which might be due to the low concentration of PMMA used in this study. The identification of PMMA-related bands in FTO/PMMA/TiO_2, wherein the polymer was subjected to 450 °C annealing, might indicate PMMA degradation. The intensity was quite similar to FTO/TiO_2, suggesting that the PMMA was no longer intact. Conversely, FTO/PMMA/TiO_2/PMMA and FTO/TiO_2/PMMA possessed higher intensity [19]. The profilometer used in this study revealed that the film thicknesses were approximately 78 ± 3.61 nm for TiO_2, 102.67 ± 6.66 nm for TiO_2/PMMA, 103 ± 8.9 nm for PMMA/TiO_2, and 128 ± 3.97 nm for PMMA/TiO_2/PMMA (averaged over three regions). These reported thickness values represent the total thickness of the deposited layers on the FTO substrate. Thus, it was hypothesized that when PMMA was heated to 450 °C while annealing TiO_2, some polymer chains might break down and depolymerize, leaving behind mostly the Monomer Methyl Methacrylate (MMA) and other volatile fragments (small hydrocarbons, CO, and CO_2) [20]. Even though the profilometer measurements after annealing demonstrated that the film thicknesses were similar (FTO/TiO_2/PMMA ≈ FTO/PMMA/TiO_2), this leftover layer was probably not made up of intact PMMA. Instead, it was likely composed of a thin, degraded, carbon-rich residue. This outcome may negatively affect the RS behavior.

AFM measurements were performed on all four stacks (Figure 6). For FTO/TiO_2, the arithmetic mean roughness (R_q) was 25.5 nm. Both FTO/PMMA/TiO_2/PMMA and FTO/TiO_2/PMMA demonstrated lower R_q values of 10.5 nm and 12.9 nm, respectively. Thus, these films were smoother than the control. The R_q (24.3 nm) of FTO/PMMA/TiO_2 resembled that of FTO/TiO_2, indicating a similar roughness trend [21]. Overall, the presence of PMMA between TiO_2 and the top electrode (carbon) might either improve or reduce the RS performance.

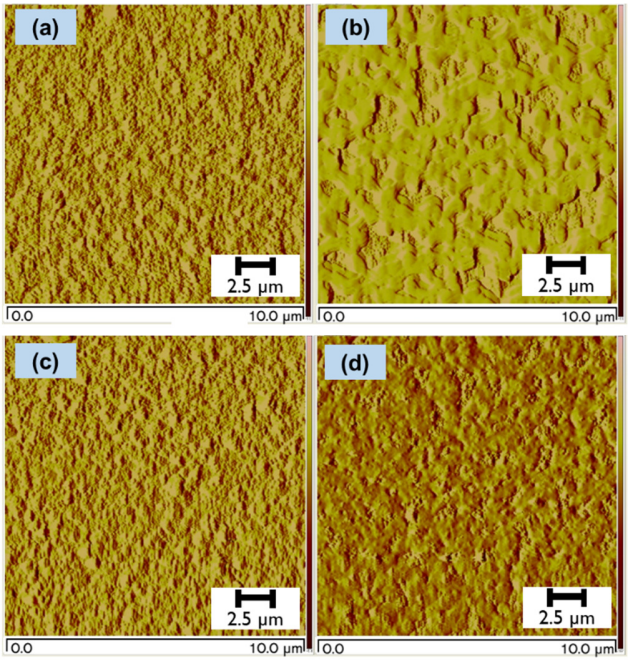

Fig. 6. AFM topography images acquired in tapping mode for: (a) FTO/TiO_2, (b) FTO/TiO_2/PMMA, (c) FTO/PMMA/TiO_2, and (d) FTO/PMMA/TiO_2/PMMA at a scan area of 10 µm × 10 µm.

B. Memory Behavior of the Fabricated TiO_2-Based Memristors Containing PMMA

The memory behaviors of the four devices with different structures were studied by running CV in the sequence of: 0 V to +6 V, +6 V to 0 V, 0 V to -6 V, and -6 V to 0 V. For the FTO/TiO_2/C, the RS pattern was unclear (Figure 7). This outcome looked rather like an ohmic conduction, suggesting that no RS behavior was recorded. Thus, FTO/TiO_2/C was not a suitable arrangement for producing memristors. Nevertheless, a sudden and weak jump of current was detected at around 3.95 V for FTO/TiO_2/PMMA/C when the voltage was swept from 0 V to +6 V. This jump indicates the switch from the High Resistance State (HRS) to the Low Resistance State (LRS), which are denoted as SET and RESET, respectively [22].

The FTO/PMMA/TiO_2/C device required a higher voltage of 5.5 V to switch on (SET) and -5.5 V to switch off (RESET). This resistance gap observed in the specific structure increased because of the insulation effect of PMMA. In contrast, the application of PMMA on top of the TiO_2 layer facilitated the smoother growth of conductive filaments [23]. Although the FTO/PMMA/TiO_2/C demonstrated a higher SET voltage, it could be beneficial for ReRAM operation by offering a greater voltage margin between the read and write processes [24]. This separation diminished the probability of read-disturb events and enhanced data stability with reliability concerning extensive memory arrays. In some cases, higher SET/RESET voltages worked better for certain high-power applications, ensuring that the filament formed more strongly [25]. No sudden increase in current was observed in the semi-logarithmic I-V curve for FTO/PMMA/TiO_2/PMMA/C, even though a large resistance gap separated the HRS (OFF) and LRS (ON). Therefore, this device did not produce any RS behavior, which could be attributed to the double addition of PMMA layers (difficult to form filamentary pathways due to the thicker PMMA/TiO_2/PMMA film). Conversely, authors in [26] reported that the gradual change in resistance suggested potential applications in analog switching for ReRAM devices. Overall, only the FTO/TiO_2/PMMA/C and FTO/PMMA/TiO_2/C devices demonstrated clear RS behaviors. Endurance tests were performed on both FTO/TiO_2/PMMA/C and FTO/PMMA/TiO_2/C over 10^2 cycles (Figure 8). For FTO/TiO_2/PMMA/C, it could retain over 10^2 cycles before breaking down. In contrast, FTO/PMMA/TiO_2/C demonstrated significantly weaker endurance, in which it could only last until the 17th cycle. When a PMMA interlayer was placed between FTO and TiO_2, their interfaces could make it harder for O^{2-} ions to move and spread out, making it harder for filaments to re-oxidize or break [27]. Although one SET/RESET might work, performing it repeatedly made switching less reliable faster.

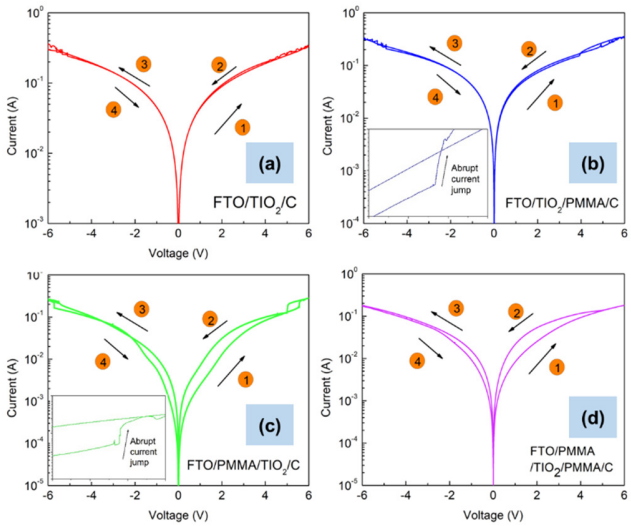

Fig. 7. The semi-logarithmic *I-V* curves (log *I* versus *V*) for: (a) FTO/TiO_2/C, (b) FTO/TiO_2/PMMA/C, (c) FTO/PMMA/TiO_2/C, and (d) FTO/PMMA/TiO_2/PMMA/C.

Figure 9 depicts the retention results established under 0.1 V read voltage for FTO/TiO_2/PMMA/C and FTO/PMMA/TiO_2/C. Both LRS and HRS supported stability that exceeded 10^4 s, with FTO/PMMA/TiO_2/C revealing weaker performance. This retention duration was comparable to previous reports for TiO_2-based ReRAM and hybrid devices [28]. The FTO/TiO_2/PMMA/C device maintained an ON/OFF ratio of 10^1, while FTO/PMMA/TiO_2/C demonstrated ratios below the 10^1 range. This outcome could be ascribed to the vacancies in TiO_2 (FTO/TiO_2/PMMA/C), which could more readily migrate under bias (filament formation likely occurred). Conversely, additional trapping, leakage, or poor vacancy mobility might occur at the PMMA/TiO_2 or FTO/PMMA interfaces for FTO/PMMA/TiO_2/C due to the degraded PMMA layer [29]. Table I outlines the obtained data for the RS parameters for all four devices, along with their standard deviation values across three devices for each structure. The FTO/TiO_2/PMMA/C was then deemed the most optimized structure.

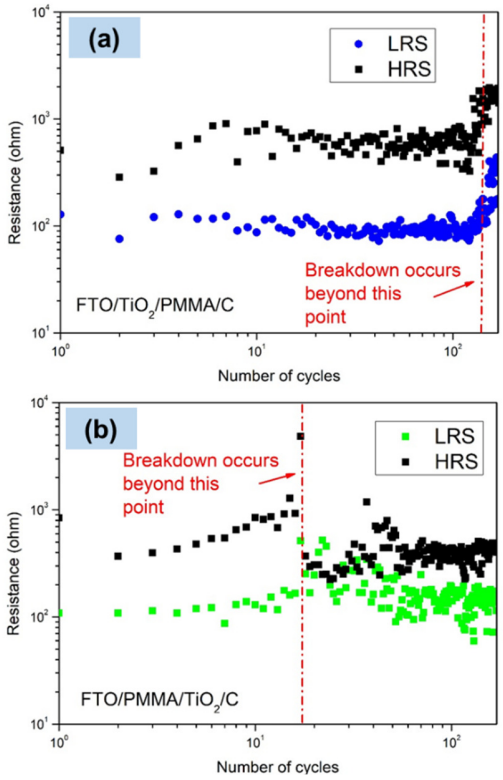

Fig. 8. The endurance tests for: (a) FTO/TiO_2/PMMA/C and (b) FTO/PMMA/TiO_2/C.

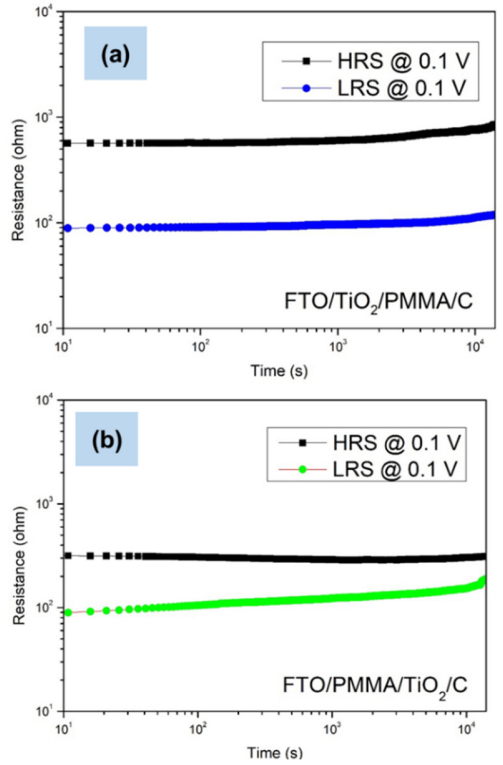

Fig. 9. The retention tests for: (a) FTO/TiO_2/PMMA/C and (b) FTO/PMMA/TiO_2/C.

TABLE I. SUMMARY OF THE OBTAINED DATA FOR THE RS PARAMETERS INVOLVING THE FOUR STRUCTURES

RS parameter	FTO/ TiO_2/C	FTO/TiO_2/ PMMA/C	FTO/PMMA/ TiO_2/C	FTO/PMMA/TiO_2/ PMMA/C
SET voltage (V_{set}, V)	-*	3.89 ± 0.29	5.38 ± 0.37	-*
RESET voltage (V_{reset}, V)	-*	-4.91 ± 0.14	-5.53 ± 0.28	-*
ON/OFF ratio	-*	~10^1	<10^1	-*
Endurance (no of cycles)	-*	~10^2	<10^2	-*
Retention (s)	-*	~10^4	~10^4	-*

Note: * = Not applicable due to absence of RS behavior.

C. *Conduction Mechanisms and Switching Dynamics of TiO_2-Based Memristors Containing PMMA*

Figure 10 shows the double logarithmic plots of the *I-V* characteristics involving the RS properties of FTO/TiO_2/PMMA/C and FTO/PMMA/TiO_2/C. Both devices displayed a distinct hysteresis loop, indicative of NVM characteristics. Initially, the devices exhibited HRS at low applied voltages, indicating the OFF state. In this region, the *I-V* curve demonstrated a linear relationship on the log-log plot with a slope of approximately 1. The linear trend suggested that conduction was regulated by an Ohmic mechanism ($I \propto V$), which was characterized by a direct proportionality between I and V [30]. Thus, the current in this state was constrained by the intrinsic concentration of the thermally generated charge carriers.

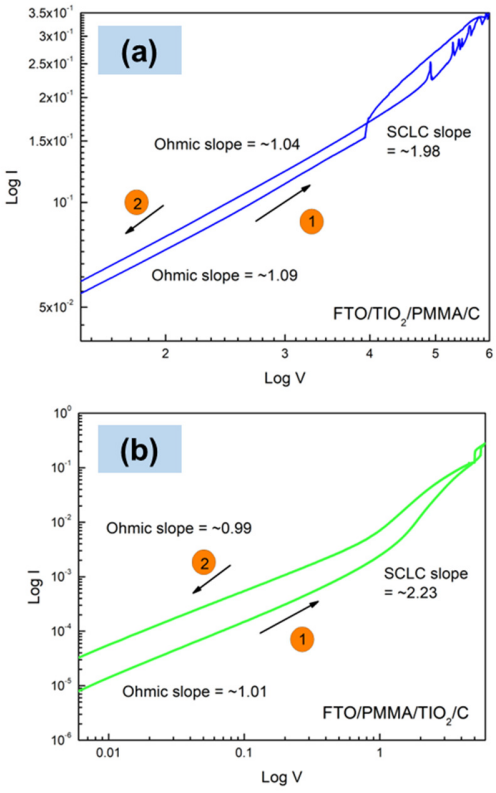

Fig. 10. The double logarithmic *I-V* curves (log I versus log V) for: (a) FTO/TiO_2/PMMA/C and (b) FTO/ PMMA/TiO_2/C.

The devices exhibited a sudden and significant increase in current, indicating the SET process with an increase in the applied voltage. This transition was marked by a significant alteration in the slope of the log-log plot, which rose to values around 2. Hence, this behavior is indicative of SCLC ($I \propto V^2$) [31]. In this regime, charge carriers were introduced from the electrodes and commenced filling trap sites within the active material, resulting in a swift rise in current. This process facilitated the formation of a conductive filament (mobile ions) that connected the anode and cathode [32]. Post-SET process, the devices maintained a stable LRS. The ongoing or reversed voltage sweep resulted in the *I-V* curve exhibiting a linear relationship with a slope near 1, signifying a reversion to Ohmic conduction.

Overall, the observed variations in the slopes and dimensions of the hysteresis loops for the two device architectures (FTO/TiO_2/PMMA/C and FTO/PMMA/TiO_2/C) indicated that the arrangement of the active layers affected the dynamics of trapping and filament formation. The observed steeper SCLC slope in the FTO/TiO_2/PMMA/C device suggested a more effective trapping and filamentary conduction process relative to the other structure, which was a characteristic advantageous for memory applications [33].

Figure 11 depicts the formation of a filamentary conduction pathway mechanism for the FTO/TiO_2/PMMA/C and FTO/PMMA/TiO_2/C. The carbon top electrode did not directly engage in the RS mechanism for FTO/TiO_2/PMMA/C and FTO/PMMA/TiO_2/C. This carbon was chemically inert and maintained stability under the applied bias compared to electrochemically active electrodes (Ag, Al, Au, and Cu, which could release mobile cations to create metallic filaments) [34].

The RS in the FTO/TiO_2/PMMA/C and FTO/PMMA/TiO_2/C structures might be determined by the migration of O^{2-} ions and the associated formation and rupture of oxygen vacancy (V_O) filaments within the TiO_2 layer [35]. This outcome suggested that the observed RS behavior was due to the intrinsic defect dynamics of the oxide. The FTO/TiO_2/PMMA/C device exhibited RS behavior mediated by the overlayer (Figure 11(a)). The PMMA overlayer functioned as an interface engineering layer, regulating the migration and accumulation of V_O at the TiO_2/PMMA interface, facilitating the controlled nucleation and growth of conductive filaments. This effect led to a more uniform, stable, and reproducible switching process compared to the control device.

The FTO/PMMA/TiO_2/C device demonstrated an insulating buffer effect, with the PMMA underlayer substantially modifying its electrical characteristics (Figure 11(b)). The switching process necessitated elevated voltages owing to the insulating properties of PMMA, which increased the device resistance and required a more robust electric field to facilitate the migration of V_O for filament formation. These increased voltages lead to higher power consumption, which is beneficial for high-density memory arrays. The FTIR results also indicated that the decomposition of PMMA at high annealing temperatures negatively affected the charge transport behavior.

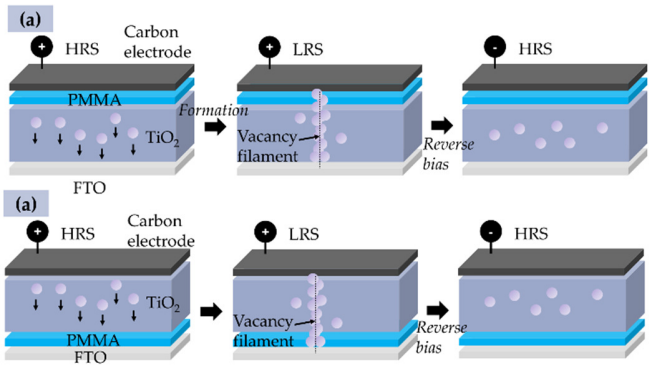

Fig. 11. The RS mechanisms of: (a) FTO/TiO_2/PMMA/C and (b) FTO/PMMA/TiO_2/C.

This original model was based solely on electrical data, indicating that structural methods are still needed to corroborate this information. Nevertheless, the electrical characteristics here matched the records of trap-mediated switching in oxide ReRAM [36]. These features entailed the *I-V* curves that were typical of transport controlled by traps with defect SCLC, a carbon top electrode that ruled out cation-driven metallic filaments, and some consistent differences within the device architectures (PMMA-altered trap density and the local electric field). The evidence supports a trap-dictated mechanism, but a distribution of VO or the filament shape would require further structural characterization, such as X-ray Photoelectron Spectroscopy (XPS), Transmission Electron Microscopy (TEM), or conductive-AFM (c-AFM).

IV. CONCLUSIONS

This study successfully demonstrated that the positioning and annealing of Polymethyl Methacrylate (PMMA) layers significantly influenced the Resistive Switching (RS) behavior of TiO_2-based memristors. The FTO/TiO_2/PMMA/C device displayed the best RS performance among all samples, with the lowest SET and RESET voltages, an ON/OFF ratio of ~10^1, a retention of ~10^4 s, and an endurance of ~10^2 cycles. This structure indicated its suitability for low-power and stable cycling applications. Overall, precise management of PMMA placement and processing conditions can optimize polymer-based hybrid structures for Resistive Random-Access Memory (ReRAM) applications. Nevertheless, future studies should focus on developing high-performance devices based on this structure, which can be suitable for industrial-scale requirements.

The results of this study indicate that the placement of PMMA is crucial in determining RS functionality in TiO_2-based memristors, rather than its mere presence. Despite earlier research indicating performance improvements from polymer incorporation, improper interfacial positioning or exposure to high-temperature annealing could hinder switching capabilities or compromise reliability. As such, for hybrid polymer-oxide ReRAM devices, a significant approach to attain low-power, solution-processed, and scalable memory technologies was presented by this design regarding interface engineering.

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