A Low-Power Low-Noise Capacitively-Coupled Chopper Instrumentation Amplifier Using a Switched Capacitor DC Servo Loop

Xuan Phuong Tran
School of Electrical and Electronic Engineering, Hanoi University of Industry, Hanoi, Vietnam
phuongtx@haui.edu.vn

Duc Dung Nguyen
School of Electrical and Electronic Engineering, Hanoi University of Industry, Hanoi, Vietnam
nguyenducdung2424@gmail.com

Duy Phong Pham
Faculty of Electronic and Telecommunication Engineering, Electric Power University, Hanoi, Vietnam
phongphd@epu.edu.vn

Manh Kha Hoang
School of Electrical and Electronic Engineering, Hanoi University of Industry, Hanoi, Vietnam
khahoang@haui.edu.vn

Xuan Thanh Pham
School of Electrical and Electronic Engineering, Hanoi University of Industry, Hanoi, Vietnam
thanhpx@haui.edu.vn (corresponding author)

Received: 24 October 2025 | Revised: 17 March 2026 and 29 March 2026 | Accepted: 9 April 2026

 DOI: https://doi.org/10.48084/etasr.15756

ABSTRACT

This paper presents a Capacitively-Coupled Chopper Amplifier (CCIA) using a Switched Capacitor DC Servo Loop (SC-DSL) to achieve low noise and low power consumption in signal amplification bandwidth for biomedical applications. The CCIA effectively mitigates the effects of mismatch and flicker noise (1/*f*). At the same time, the SC-DSL maintains a balanced electrode bias at the input and facilitates the efficient amplification of signals, such as Electrocardiography (ECG) and Electroencephalography (EEG), free from interference caused by variations in electrode material and size. The simulation results, utilizing 180 nm CMOS technology, indicate that the proposed design occupies an area of 0.04 mm². The CCIA has a low power consumption of 1.75 µW and low Input-Referred Noise (IRN) of 1.02 µV_{rms} from a voltage supply of 1 V. By using the SC-DSL, the CCIA can be operated with an input electrode offset of up to 50 mV. Furthermore, the operational bandwidth attained 7.64 kHz.

Keywords-CCIA; low noise; electrode offset; DC servo loop; switched-capacitor

I. INTRODUCTION

The progression of integrated circuit manufacturing technology has improved accessibility in personalized healthcare, enabling early diagnosis and successful treatment of diseases through accurate recording and identification of bio-signals [1]. Electroencephalograms (EEG) and Electrocardiograms (ECG) exhibit low amplitude, generally ranging from tens of microvolts (µV) to several millivolts (mV), with a frequency range spanning from 0.5 Hz to 150 Hz [2]. Amplifiers for bio-signal recording systems must exhibit elevated input impedance, significant gain, little input noise, low power consumption, and a compact form factor [3]. Therefore, bio-signals need amplification before the next processing steps.

In order to achieve low power and low noise, the Capacitively-Coupled Chopper Amplifier (CCIA) is used [3, 4]. The DC offset originates from biological electrodes, especially the common wet electrodes, which can cause fluctuations of up to 50 mV in the DC voltage due to differing skin contact conditions [5]. The input electrode offset voltage

(VEOS) can lead to a significant common-mode voltage imbalance, resulting in output saturation. Certain methods have been proposed to eliminate the DC voltage offset. In [6-8], a pseudo-resistor using a PMOS transistor was employed to provide a high-pass filter. However, technical faults in the design process often result in significant nonlinearity in the dummy resistor, consequently greatly affecting signal quality. The offset voltage is reduced by programming and regulating an external capacitor array [9]. This structure fails to meet the device standards for applications [3]; therefore, the optimal choice is to execute a DC Servo Loop (DSL) [6, 10]. In the conventional pseudo-resistor DSL, the large resistance required for sub-Hz high-pass filtering introduces significant thermal noise ($\overline{v_n^2} = 4kTR_{eq} \times BW$), which becomes the dominant noise source in the sub-100 Hz band [11]. Authors in [12] promoted the use of pseudo-resistors to achieve significant equivalent resistance in a confined area. However, the pseudo-resistors introduce considerable nonlinearity and contribute thermal noise to the system [13], as demonstrated in [6-8], thus affecting the signal. To mitigate the nonlinearity introduced by the pseudo-resistor and optimize the design area, the present study utilizes a series-connected Switched Capacitor Resistor (SC-R) configuration. Moreover, the proposed Switched Capacitor DC Servo Loop (SC-DSL) replaces the pseudo-resistor with a switched-capacitor network, which provides an equivalent large resistance without a physical noisy resistor. The only added noise from the SC network arises from the sampling switches (kT/C noise), which can be designed to be negligible by choosing capacitances large enough. Machine learning techniques have been integrated into a wide range of applications. For instance, authors in [14] applied such techniques to optimize pseudo-resistors, yielding significant benefits. Extending this concept, ML algorithms could be employed to dynamically calibrate the proposed SC-DSL, adaptively tuning the high-pass corner frequency or compensating for process and temperature variations to further enhance robustness and linearity. This approach is expected to see widespread adoption/be widely adopted in future designs.

This work proposes and analyzes the fluctuations of the SC-R's equivalent resistance with respect to frequency, capacitor value, switch impedance, and temperature. When the SC-DSL is activated, the CCIA can amplify biomedical signals while preventing VEOS of up to 50 mV.

II. DESIGN

Figure 1 shows the proposed design, which includes two loops - a negative feedback loop and a DSL - as well as a CCIA primary path. The primary path amplifier comprises two amplification stages that achieve significant gain and substantial output swing. In the initial stage, referred to as G_{m1}, a Folded Cascode (FC) configuration is utilized with a bias current of 0.7 µA. This arrangement provides significant amplification while improving circuit efficiency and enabling current reutilization. In the second amplification stage, a differential amplifier, G_{m2}, is utilized in conjunction with a pair of resistors, $R_{S1,2}$ = 280 kΩ, and capacitors, $C_{S1,2}$= 500 fF, for stable operation. The input capacitors $C_{in1,2}$ possess a capacitance of 5 pF, whereas the negative feedback capacitors $C_{fb1,2}$ have a capacitance of 50 fF. The closed loop gain A_V is defined by the ratio C_{in}/C_{fb}, resulting in a gain of 40 dB. To reduce the design space and achieve high impedance, a common mode voltage $V_{CM} = V_{DD}/2 = 0.5$ V is utilized to bias G_{m1} via the NMOS pseudo-resistors $R_{b1,2}$ with a supply voltage V_{DD} of 1 V. Figure 1 demonstrates the configuration of the chopper, comprising four MOSFET switches. These switches are controlled by two clocks, $\Phi_{p,n}$. When the input signal Vin passes through the input chopper (CH_{in}), it modulates to a high frequency. Then, after passing through G_{m1}, the signal is amplified and demodulated to the base frequency band after passing through the output chopper (CH_{out}). The noise generated by G_{m1} is eliminated because it is modulated outside the CCIA's bandwidth, while the biomedical input signal remains amplified. The intrinsic offset voltage of G_{m1}, denoted as V_{OS}, arises from the effects of manufacturing mismatch. The amplification effect of V_{OS} by G_{m1} produces a significant offset voltage at the output of the first stage. The offset voltage modulated by the chopper output (CH_{out}) will generate an output ripple, thus significantly affecting the output. To mitigate the impact of V_{OS} at the output, DC blocking capacitors $C_{b1,2}$ = 1 pF are positioned following G_{m1}.

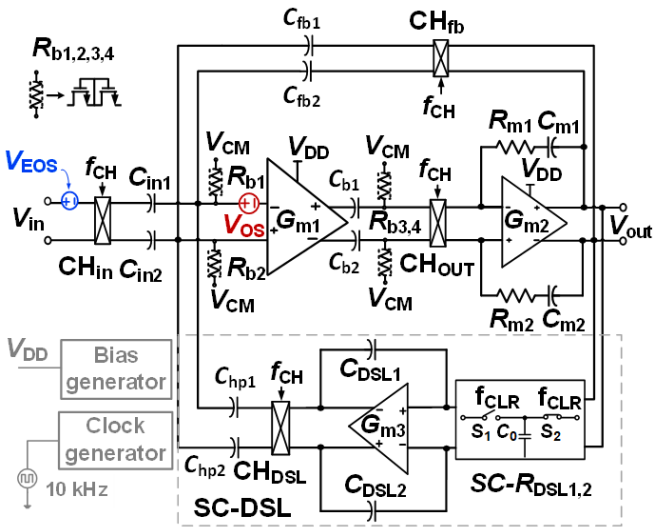

Fig. 1. Schematic of the proposed CCIA with SC-DSL.

At the input node, a DC electrode offset (V_{EOS}) is generated due to the mismatched size and differing materials of the contact tissues. The V_{EOS} can reach 50 mV above the biological signal. This voltage causes amplifier saturation. The proposed design incorporates an SC-R due to the utilization of the chopper approach in the SC-DSL. The SC-DSL consists of an integrator to amplify the low-frequency signal at the CCIA's output node, a high-pass chopper (CH_{hp}) to modulate the amplified low-frequency signal, and capacitors $C_{hp1,2}$ to convert voltage into current. The integration procedure will continue until the output signal of the CCIA is free of DC components. The combination of the transfer function V_{out}/ V_{in} and the transfer function of the DSL integrator produces a high-pass corner frequency defined as:

$$f_{hp} = \frac{C_{hp1,2}}{C_{fb1,2}} \times f_{SC\text{-}DSL} \quad (1)$$

where $C_{hp1,2}$ and $C_{fb1,2}$ are the DSL output and feedback capacitors of the CCIA, respectively, and $f_{SC\text{-}DSL}$ is the cutoff frequency determined by the SC-DSL loop following the equation $f_{SC\text{-}DSL} = 1/2\pi \times (R_{SC\text{-}DSL1,2} \times C_{SC\text{-}DSL1,2})$. Consequently, the impact of V_{EOS} will be eliminated at the output of the SC-DSL. Significant values are frequently required for the input resistors of integrators in SC-DSL. This paper proposes an SC-R arrangement to mitigate the effects of mismatch and drawbacks of the pseudo-resistors.

III. IMPLEMENTATION

The first stage of CCIA, G_{m1}, employs an FC with Common-Mode Feedback (CMFB) circuits, often used in integrated circuits, as illustrated in Figure 2. The G_{m1} amplifier features a symmetrical design that includes a differential input stage and a cascode stage, enabling the achievement of high gain and wide bandwidth. A CMFB circuit is utilized for maintaining a constant output voltage of $V_{CM} = V_{DD}/2$. This configuration generates and supplies the V_{CMFBL} voltage to the gate terminals of transistors M_{10} and M_{11}. Figure 2 displays the sizing of the MOSFET devices in the FC and CMFB circuits. Figure 3 depicts the schematic of G_{m2}, integrated with the phase margin enhancement components, $C_{m1,2}$ and $R_{m1,2}$. The network, constructed from the resistors $R_{S1,2}$ and capacitors $C_{S1,2}$, is utilized to determine the common voltage [15]. The resistors $R_{S1,2}$, utilized in this design, include pseudo-resistors configured as two diodes [16], while the MIM capacitors $C_{S1,2}$ are connected in parallel with $R_{S1,2}$. The parameters of the CMOS transistors in G_{m2} are, likewise, portrayed in Figure 3.

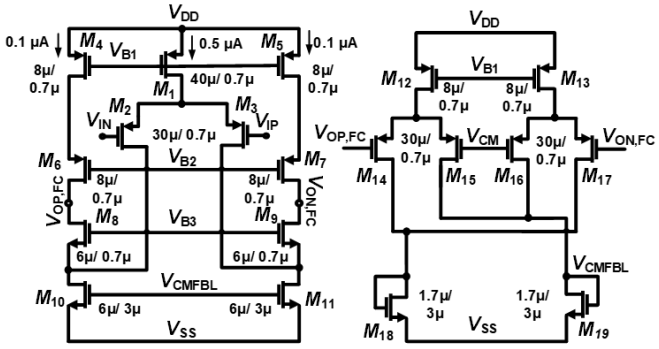

Fig. 2. Schematic of FC amplifier (G_{m1}) and CMFB circuit.

Figure 4 shows a two-stage amplifier in the SC-DSL, which is biased for ultra-low current consumption. The first stage is a differential amplifier, whereas the second stage is a common-source amplifier. The CMFB circuit in the SC-DSL ensures that the output voltage is maintained at $V_{CM} = V_{DD}/2$. The Miller capacitors $C_{CD1,2}$ of 500 fF and the resistors $R_{CD1,2}$ of 280 kΩ are utilized to stabilize the amplifier's operation. Figure 4 exhibits the dimensions of the MOS transistors of the two-stage amplifier in SC-DSL.

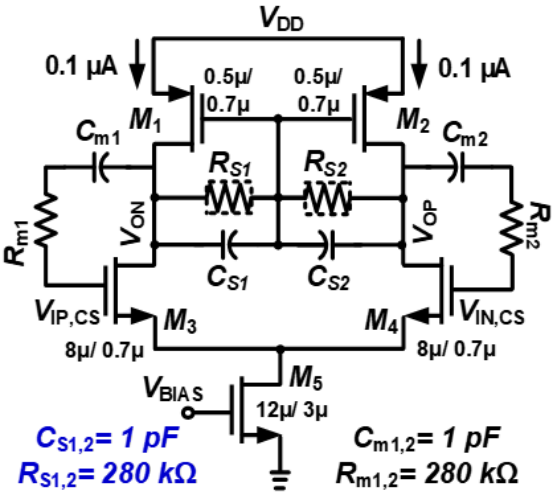

Fig. 3. Schematic of common-source (G_{m2}).

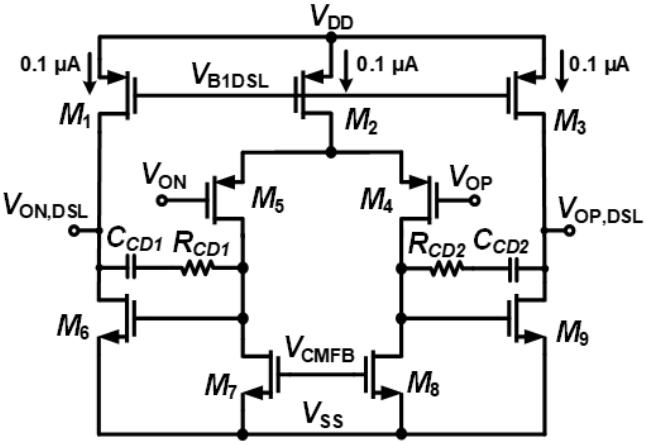

Fig. 4. Schematic of intergrator with $R_{CD1,2}$ = 280 KΩ and $C_{CD1,2}$ = 500 fF.

The proposed SC-R, depicted in Figure 5, consists of two switches controlled by two out-of-phase clock signals, Φ_p and Φ_n, together with four capacitors, comprising two capacitors C_1 and two capacitors C_2. The equivalent resistance can be determined as:

$$R_{eq} = \frac{k \times (k^2 \times C_1 + C_2)}{f_{CLR} \times C_1 \times C_2} \quad (2)$$

where k represents the number of SC pairs in the array, and f_{CLR} denotes the frequency signal supplied to switches S_0-S_8. If k is significantly greater than 1, then $k \times C_1$ is significantly greater than C_2, allowing (2) to be simplified to:

$$R_{eq} = \frac{k^3}{f_{CLR} \times C_1} \quad (3)$$

This shows that the equivalent resistance grows with the cube of k. Thus, k is a key design parameter that allows large resistances to be realized using a modest number of capacitor pairs without requiring physically large on-chip resistors. The implementation uses the series-parallel charge sharing

mechanism in the unit capacitor with a capacitance of $C_1 = C_2 = C_0 = 50$ fF. Nonetheless, the existence of parasitic effects on the capacitor, along with the clock switching enabled by the switches, may lead to alterations in the equivalent resistance. The present work will investigate the variations in resistance values of the proposed SC-R network due to alterations in clock frequency or switch dimensions, to evaluate their impact on system performance.

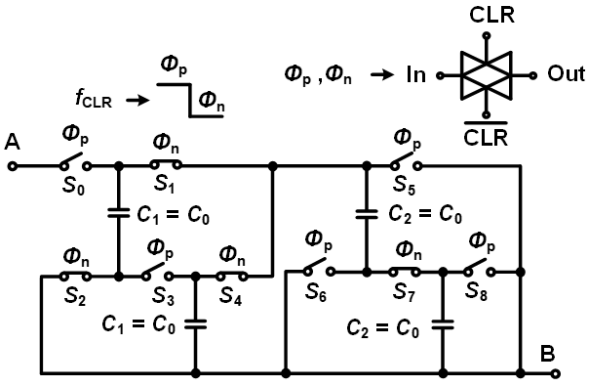

Fig. 5. Schematic of the proposed SC-R.

Figure 6 demonstrates the relationship between the SC-R resistance and the clock frequency f_{CLK}. With a 50% duty cycle and frequency swept from 1 to 8 kHz, a discrepancy is observed between the theoretical resistance (3) and the simulation results. This deviation is attributed to non-idealities, such as MOSFET switch imperfections, parasitic capacitances, and second-order effects, not accounted for in the ideal equation. Figure 7 shows the relationship between the C_0 value and the SC-R resistance value. Moreover, as indicated by (3), the resistance value of SC-R has an inverse correlation with C_0, emphasizing the interdependence of resistance on both frequency and capacitance within the system. As the capacitance C_0 rises, the equivalent resistance of the entire structure diminishes, signifying an inverse correlation between C_0 and the equivalent resistance. This association aligns with (3). The utilization of MOSFET switches results in mismatches, while parasitic elements in the capacitors create a disparity between the theoretical and actual resistance levels.

Equation (3) indicates that at a control frequency of $f_{CLR} = 5$ kHz and $C_0 = 50$ fF, the anticipated equivalent resistance of SC-R is 40 GΩ. Nevertheless, as illustrated in Figure 7, under identical conditions, the recorded resistance is merely 9.7 GΩ and diminishes further with an increase in C_0. This discrepancy results not only from parasitic effects but also from the mismatch between the MOSFETs and the implications of the switching process. Improving charge accumulation facilitates more efficient current transfer, hence reducing power dissipation and circuit resistance. In the proposed SC-R configuration (Figure 5), the switches Φ_p and Φ_n utilize a Transmission Gate (TG) to reduce resistance relative to using a single MOSFET switch. Figure 8 demonstrates that the equivalent resistance of the structure is directly affected by the resistance of the switch. Consequently, the dimensions of the MOSFET utilized in the switch significantly influence the SC-R value. In examining the impact of switch sizing on SC-R resistance, the Length (L) of the MOS switches is analyzed in three scenarios: 0.3, 0.5, and 1 µm, revealing that as the width increases, the equivalent resistance tends to decrease. The inherent resistance of the switch is exactly proportional to the width-to-length ratio. Consequently, when the width increases, the internal resistance of the switch decreases, leading to a decrease in the total equivalent impedance of the system. Figure 9 presents the simulated value of the SC-R as a function of transistor width, plotted for three distinct temperatures: –40 °C, 27 °C, and 70 °C. As the temperature increases, the effective resistance decreases consistently across all device widths. For instance, at a width of 1 µm, the resistance drops from approximately 19.5 GΩ at –40 °C to 4.5 GΩ at 70 °C. This inverse relationship is primarily attributed to temperature-dependent carrier mobility and threshold voltage variations in the MOS devices. Figure 10 displays the Monte Carlo simulation of the SC-R with a mean value of 9.38 GΩ and a low standard deviation of 0.18 GΩ. The simulation results indicate that the SC-R exhibits high linearity. The narrow Gaussian distribution confirms that the resistance is well-controlled and largely immune to random process variations.

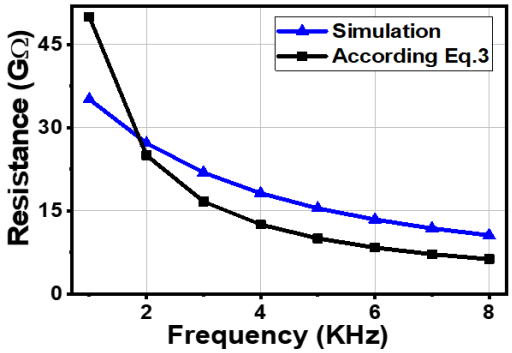

Fig. 6. Value of SC-$R_{DSL1,2}$ when f_{CLR} frequency changes.

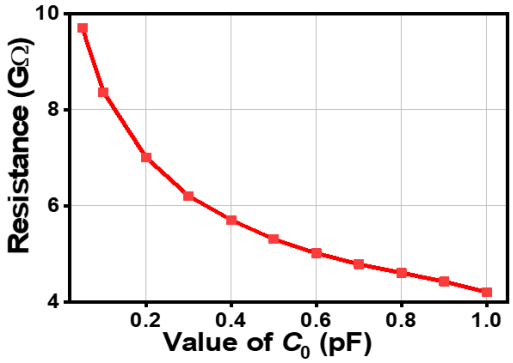

Fig. 7. Value of SC-$R_{DSL1,2}$ when the capacitor C_0 changes.

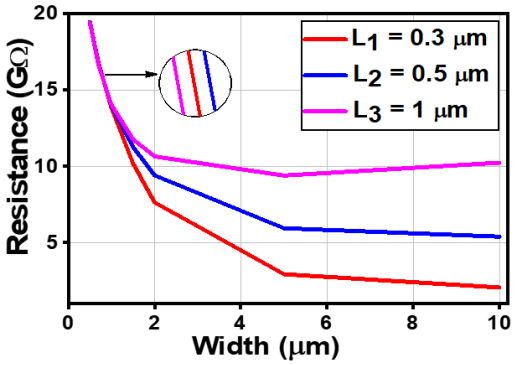

Fig. 8. Value of SC-R when the length and width of the switch change.

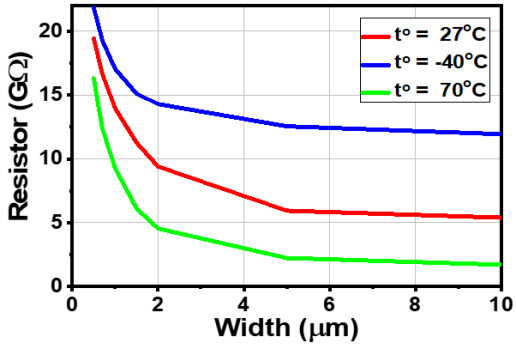

Fig. 9. Value of SC-R with temperature variation.

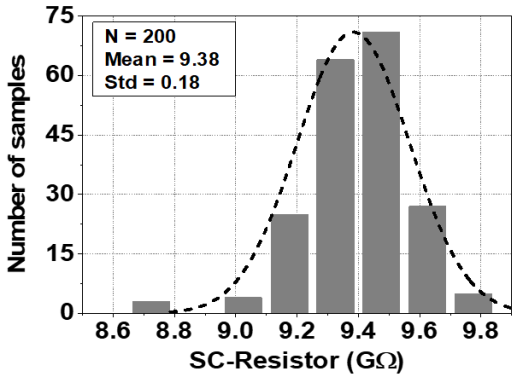

Fig. 10. The Monte Carlo simulation results of SC – R resistance.

IV. SIMULATION RESULTS

By using CMOS 180 nm technology, the layout of the proposed design occupies an area of around 0.04 mm², as shown in Figure 11. The results are derived from post-layout simulations that incorporate foundry-provided models, including parasitic (RCC) extractions from the complete layout. The simulated transfer function of the proposed design, presented in Figure 12, demonstrates a well-defined bandpass response with a measured bandwidth of 8.2 kHz. This passband enables the circuit to process a wide range of signal frequencies while maintaining signal integrity. The lower cutoff is established by a high-pass corner frequency (f_{hp}) of 0.56 Hz, which is actively set when the SC-DSL is enabled to suppress low-frequency noise and interference. The circuit achieves a closed-loop gain of approximately 40 dB within the passband. This gain magnitude is sufficient to amplify weak biomedical signals while the high-pass characteristic effectively rejects the DC electrode offset voltage V_{EOS} at the input, preventing saturation and ensuring robust operation.

The simulation results of CMRR and PSRR of the proposed CCIA, portrayed in Figure 13, validate that the proposed design achieves superior interference rejection metrics. With CMRR exceeding 118 dB and PSRR exceeding 100 dB across the entire passband, the circuit demonstrates the ability to extract weak differential bio-signals while effectively suppressing both common-mode environmental noise and power supply disturbances.

Figure 14 shows the Input-Referred Noise (IRN) of the proposed circuit, which exhibits a thermal noise floor of approximately 62 nV/$\sqrt{\text{Hz}}$. A key feature of the noise spectrum is the transition between low-frequency and high-frequency regimes, marked by the 1/*f* noise corner frequency. This corner occurs at 10 Hz, indicating the point at which flicker noise (1/*f* noise) begins to dominate over thermal noise. The use of the chopper stabilization technique effectively attenuates the 1/*f* noise, significantly reducing its contribution to the overall noise performance. The integrated IRN is approximately 0.96 μV_{rms}, highlighting the circuit's capability for low-noise operation. Figure 15 presents a detailed breakdown of the power consumption of the Capacitively-Coupled Instrumentation Amplifier (CCIA). Total power consumption is approximately 1.75 μW from a 1 V supply. Within the SC-DSL, transconductance stages G_{m1}, G_{m2}, and G_{m3} consume 54.28%, 11.44%, and 17.14% of the total power, respectively, while the bias circuit accounts for the remaining 17.14%. Figure 16 depicts the simulated result of the transient behavior of the CCIA's output V_{out}. The amplifier is driven by a 1 mV input signal V_{in}, which is representative of the amplitude of typical biomedical signals (such as ECG or EEG).

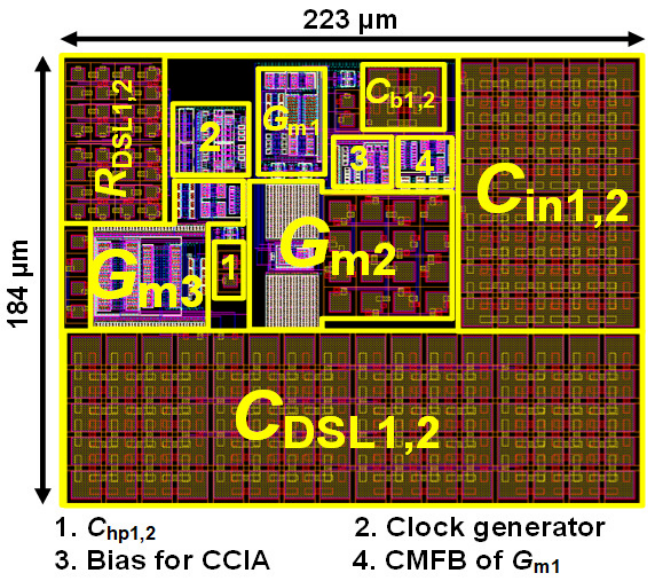

Fig. 11. Layout of the proposed CCIA.

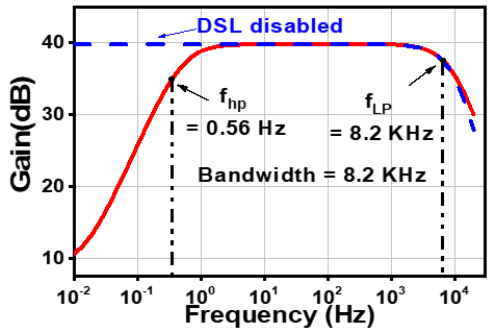

Fig. 12. Simulated result of the proposed CCIA's frequency response.

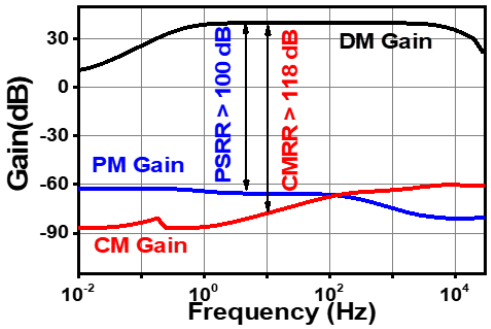

Fig. 13. Simulated results of CMRR and PSRR of the proposed CCIA.

Table I provides a comprehensive benchmark of the proposed amplifier against [17-21], evaluating key metrics essential for biomedical front-end applications, including process technology, power efficiency, noise performance, and interference rejection. In terms of technology, this work employs a 180 nm process, consistent with [17, 18]. This node offers a favorable balance between cost, leakage current, and analog performance. Operating from a 1 V supply, the proposed circuit dissipates only 1.75 µW. This power consumption is lower than that of [17] (8.3 µW), [19] (6.3 µW), [20] (5.4 µW), and [21] (2.8 µW). While [18] achieves a slightly lower power draw of 1.1 µW, it does so at the expense of significantly degraded CMRR and noise performance. The proposed design achieves a CMRR greater than 118 dB, the highest among all compared works. This surpasses [17] (117 dB), [19] (112 dB), [20] (110 dB), and substantially outperforms [18] (40 dB) and [21] (78 dB). Such exceptional common-mode rejection ensures robust suppression of interference, such as power-line noise, in challenging environments. The Power Efficiency Factor (PEF) serves as a key figure of merit, combining noise, power, and bandwidth, where a lower value indicates superior efficiency. This work attains a PEF of 12, the lowest in the comparison conducted, outperforming [17] (56.85), [18] (29), [19] (52.8), [20] (15.5), and [21] (65.7). This result demonstrates that the proposed design achieves an optimal trade-off among low noise, low power consumption, and wide bandwidth, making it highly suitable for energy-constrained biomedical applications.

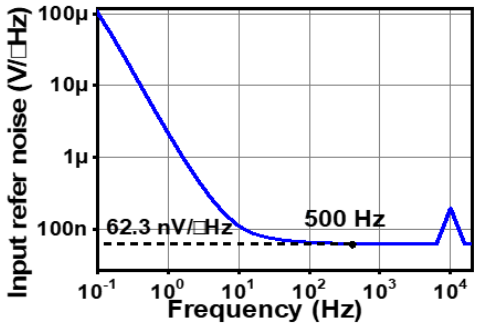

Fig. 14. Simulated IRN of the CCIA.

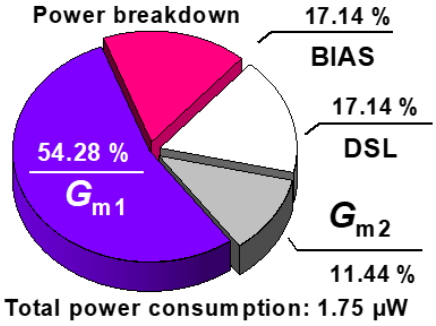

Fig. 15. Power consumption of the proposed CCIA.

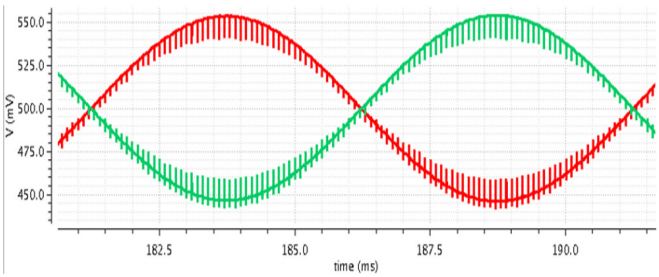

Fig. 16. The simulated result of the transient behavior of the CCIA's output V_{out} when V_{in} = 1 mV.

TABLE I. PERFORMANCE COMPARISON

Specs.	**Similar works**					**This work**
	[17]	**[18]**	**[19]**	**[20]**	**[21]**	
Process (nm)	180	180	130	65	40	180
Supply (V)	1.8	1.2	2	1.2	1.2	1
Area (mm^2)	0.026	0.011	0.6	N/A	0.071	0.04
Power (µW)	8.3	1.1	6.3	5.4	2.8	1.75
BW (kHz)	7.3	10	0.32	0.25	5.0	8.2
f_{hp} (Hz)	Y	Y	Y	Y	Y	Y
C_{in} (pF)	7.6	1.5	N/A	32	1	5
CMRR (dB)	117	40	112	110	78	>118
PSRR (dB)	88	N/A	101	N/A	76	>100
IRN (µV_{rms}) (1-200 Hz)	0.96	12.7	2.4	0.44	1.8	0.96
PEF	56.85	29	52.8	15.5	65.7	12

V. CONCLUSIONS

This paper introduces a Capacitively-Coupled Instrumentation Amplifier (CCIA) and a Switched Capacitor DC Servo loop (SC-DSL) that uses a Switched Capacitor Resistor (SC-R). It is all built in 180 nm technology and is used in biomedical applications. To mitigate the VEOS, the proposed SC-DSL incorporates an SC-R to eliminate thermal noise, while still amplifying biological signals such as Electrocardiography (ECG) and Electroencephalography (EEG) within the CCIA. Simulations performed with 180 nm CMOS technology show that the proposed design needs only 0.04 mm² of area. The CCIA has a minimal power consumption of 1.75 µW and a low Input-Referred Noise (IRN) of 0.96 μV_{rms}, operating from a voltage supply of 1 V. The SC-DSL allows the CCIA to operate with an input electrode offset of up to 50 mV. Moreover, the working bandwidth reaches 7.64 kHz.

DECLARATION OF COMPETING INTERESTS

The author declares that there are no competing interests.

ACKNOWLEDGMENT

This research received no external funding.

DATA AVAILABILITY

The data supporting the findings of this study are available from the author upon reasonable request.

REFERENCES

[1] X. T. Pham, X. T. Kieu, and M. K. Hoang, "Ultra-Low Power Programmable Bandwidth Capacitively-Coupled Chopper Instrumentation Amplifier Using 0.2 V Supply for Biomedical Applications," *Journal of Low Power Electronics and Applications*, vol. 13, no. 2, 2023, Art. no. 37, https://doi.org/10.3390/jlpea13020037.

[2] K. Xu, Y. Yang, Y. Li, Y. Zhang, and L. Zhang, "A High-Performance System for Weak ECG Real-Time Detection," *Sensors*, vol. 24, no. 4, 2024, Art. no. 1088, https://doi.org/10.3390/s24041088.

[3] L. Balla and V. K. S. Gollakota, "A Low Noise Amplifier with 27 dB Gain and 1.78 dB Noise for Satellite Communications with 0.1 µm GaAs pHEMT Technology," *Engineering, Technology & Applied Science Research*, vol. 13, no. 5, pp. 11763–11767, Oct. 2023, https://doi.org/10.48084/etasr.6264.

[4] X. T. Pham, X. P. Tran, K. V. Nguyen, V. T. Le, D. P. Pham, and M. K. Hoang, "A 1.9 µW 127 n V/ √Hz Bio Chopper Amplifier Using a Noise-Efficient Common Mode Cancelation Loop," in *2022 International Conference on Advanced Technologies for Communications* (*ATC*), Ha Noi, Vietnam, Oct. 20–22, 2022, pp. 116–120, https://doi.org/10.1109/ATC55345.2022.9942987.

[5] G. Texis-Texis *et al*., "Development of a Prototype for the Acquisition of Biopotentials Implementing a New Interconnection Method for Shielding," *Applied Sciences*, vol. 15, no. 5, 2025, Art. no. 2442, https://doi.org/10.3390/app15052442.

[6] Y.-K. Huang and S. Rodriguez, "Noise Analysis of Current-Feedback DC-Servo Loop in Current-Balancing Chopper Amplifiers," in *2022 IEEE Nordic Circuits and Systems Conference* (*NorCAS*), Oslo, Norway, Oct. 25–26, 2022, pp. 1–6, https://doi.org/10.1109/NorCAS57515.2022.9934347.

[7] F. Karami Horestani and J. M. de la Rosa, "Ultra-High-Resistance Pseudo-Resistors With Small Variations in a Wide Symmetrical Input Voltage Swing," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 8, pp. 2794–2798, Aug. 2023, https://doi.org/10.1109/TCSII.2023.3258880.

[8] K. Wen, S. Liu, L. Zhong, Y. Shen, and Z. Zhu, "A −64.3 dB THD, 26 nV/√ Hz Bio-Potential Readout Analog-Front-End Amplifier With a Gm-C Integrator-Implanted DC Servo Loop, and a Bulk-Driven Ripple Reduction Loop," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 71, no. 2, pp. 537–547, Feb. 2024, https://doi.org/10.1109/TCSI.2023.3329805.

[9] J. Cuenca, B. Zambrano, E. Garzón, L. M. Prócel, and M. Lanuzza, "An Accurate and Low-Complexity Offset Calibration Methodology for Dynamic Comparators," *Journal of Low Power Electronics and Applications*, vol. 15, no. 2, 2025, Art. no. 35, https://doi.org/10.3390/jlpea15020035.

[10] C. Zhang, J. Wang, L. Wang, L. Liu, Y. Li, and Z. Zhu, "High Input Impedance Low-Noise CMOS Analog Frontend IC for Wearable Electrocardiogram Monitoring," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 7, pp. 1169–1173, July 2020, https://doi.org/10.1109/TCSII.2019.2932463.

[11] L. Liu, T. Hua, Y. Zhang, J. Mu, and Z. Zhu, "A Robust Bio-IA With Digitally Controlled DC-Servo Loop and Improved Pseudo-Resistor," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 3, pp. 440–444, Mar. 2020, https://doi.org/10.1109/TCSII.2019.2922423.

[12] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. New York, NY, USA: McGraw-Hill Companies, 2016.

[13] L. G. Salem, "Analysis and Optimization of Switched-Capacitor Piezoelectric Energy Harvesting Interface Circuits," *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, vol. 31, no. 9, pp. 1389–1402, Sept. 2023, https://doi.org/10.1109/TVLSI.2023.3284429.

[14] M. A. Farshori *et al*., "Novel Tunable Pseudoresistor-Based Chopper-Stabilized Capacitively Coupled Amplifier and Its Machine Learning-Based Application," *Micromachines*, vol. 16, no. 9, 2025, Art. no. 1000, https://doi.org/10.3390/mi16091000.

[15] F. Ansari and M. Yavari, "A High Input Impedance Fully-Differential Chopper Amplifier for Closed-Loop Neural Recording," in *28th Iranian Conference on Electrical Engineering* (*ICEE*), Tabriz, Iran, Aug. 04–06, 2020, pp. 1–5, https://doi.org/10.1109/ICEE50131.2020.9260657.

[16] F. M. Yaul and A. P. Chandrakasan, "A Noise-Efficient 36 nV/ \surd Hz Chopper Amplifier Using an Inverter-Based 0.2-V Supply Input Stage," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 3032–3042, Nov. 2017, https://doi.org/10.1109/JSSC.2017.2746778.

[17] Z. Zhou *et al*., "A High CMRR Instrumentation Amplifier Employing Pseudo-Differential Inverter for Neural Signal Sensing," *IEEE Sensors Journal*, vol. 22, no. 1, pp. 419–427, Jan. 2022, https://doi.org/10.1109/JSEN.2021.3130003.

[18] K. Ann Ng, L. Zhang, H. Wu, T. Tang, and J. Yoo, "A Single-Stage, Capacitively-Coupled Instrumentation Amplifier With Complementary Transimpedance Boosting," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 71, no. 7, pp. 2989–3001, July 2024, https://doi.org/10.1109/TCSI.2024.3391169.

[19] Y.-P. Hsu, Z. Liu, and M. M. Hella, "A −68 dB THD, 0.6 mm² Active Area Biosignal Acquisition System With a 40–320 Hz Duty-Cycle Controlled Filter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 1, pp. 48–59, Jan. 2020, https://doi.org/10.1109/TCSI.2019.2943904.

[20] U. Ha, J. Lee, M. Kim, T. Roh, S. Choi, and H.-J. Yoo, "An EEG-NIRS Multimodal SoC for Accurate Anesthesia Depth Monitoring," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 6, pp. 1830–1843, June 2018, https://doi.org/10.1109/JSSC.2018.2810213.

[21] H. Chandrakumar and D. Marković, "An 80-mVpp Linear-Input Range, 1.6- GΩ Input Impedance, Low-Power Chopper Amplifier for Closed-Loop Neural Recording That Is Tolerant to 650-mVpp Common-Mode Interference," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2811–2828, Nov. 2017, https://doi.org/10.1109/JSSC.2017.2753824.