Dynamic Simulation and Harmonic Evaluation of a Hybrid Multilevel Inverter for Photovoltaic Systems Using Pulse Width Modulation Strategies

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ABSTRACT

The current work proposes a novel design of Cascaded H-bridge (CHB) and half-bridge for an asymmetric hybrid Multi-Level Inverter (MLI) to generate a nine-level output using a reduced number of power switches. By utilizing three unequal DC voltage sources, the proposed topology achieves an extended range of nine-level output voltages while maintaining a simplified and compact architecture. A comprehensive evaluation of the proposed asymmetric MLI was conducted, namely, the cost function, component count per level, and total standing voltage. The output performance of the proposed MLI was evaluated using three carrier-based Pulse Width Modulation (PWM) techniques: Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition (APOD), and by simulating in MATLAB Simulink a Photovoltaic (PV) system under variable irradiance. The simulation results revealed that the PD technique demonstrated superior performance in achieving the lowest Total Harmonic Distortion (THD) of 13.98% at a modulation index of 0.95. A comparative analysis was performed with other existing topologies. The proposed topology achieved a Total Standing Voltage per unit (TSV_{PU}) of 18 V_{DC} and cost function values of 4.75 and 6.25, while the total component count per level was calculated as 1.67, which is comparatively lower than that of the existing topologies. In conclusion, the reduction of the switch count significantly decreases the switching losses, system complexity, and installation costs compared to traditional MLI configurations.

Keywords-multilevel inverter; pulse width modulation; photovoltaic system; total harmonic distortion

I. INTRODUCTION

The use of fossil fuels has increased as a result of the rising global energy consumption, which has a detrimental effect on the ecosystem by releasing greenhouse gases into the atmosphere. Therefore, renewable energy resources have attracted increased interest. PVs are one of the fastest-growing energy sources owing to their affordability, accessibility, and widespread applications. Most solar panels today have an efficiency of only 15% to 20%, and this energy must be transformed into electrical energy for utility use. PVs can produce electricity efficiently and with minimal pollution [1]. Multi-Level Inverters (MLIs) convert DC to AC using multiple voltage levels, improving the output quality and reducing harmonics. The first MLI was introduced in 1975. Since then, a lot of research has been conducted on DC-AC power conversion using MLI and its applications, such as active filters, flexible AC transmission systems, power factor correction, uninterruptible power supplies, static VAR compensators, and high-voltage DC power transmission.

High input current and output voltage values are the primary causes of inverter losses. Thus, the most efficient inverters must be designed to maximize the energy that may be

obtained from renewable sources, such as solar cells [2]. The significant benefits of MLI include lower switching frequency and switching losses, reduced overall harmonic distortion, enhanced power quality with strong electromagnetic compatibility, and lower voltage stress on switches. Using commonly available low-medium voltage semiconductors, an increased number of levels can be generated [3]. In general, MLIs have multiple advantages, but typically employ a large number of switches, which directly increases the overall losses and cost of the inverter. Essentially, there are three types of MLI structures: CHB, Flying Capacitor (FC), and Diode Clamped or Neutral Point Clamped (NPC) [4].

Several researchers have been working to reduce the overall size and cost of MLIs. Using switches and other techniques, a topology with a lower blocking voltage was proposed to calculate the total amplitude of the DC voltage source [5]. Based on the DC voltage magnitudes, the CHB inverter is divided into symmetric and asymmetric types and consists of multiple single-phase H-bridge topologies. Each topology has advantages and disadvantages related to complexity, cost, and performance. The asymmetric type's modularity is preserved by non-identical DC sources that require fewer switches to produce higher voltage levels [6]. In [7], a 9-level CHB-MLI using 12 switches with variable DC sources was presented, aiming to reduce THD and improve efficiency by selecting optimal voltage levels. Although the proposed approach enhanced the waveform quality, the main drawback was the increased number of switches, which increased the system complexity and cost. Authors in [8] evaluated the harmonic reduction in diode-clamped and cascaded MLIs using various Pulsed Width Modulation (PWM) techniques. The modified reference and carrier PWM method achieved the lowest THD, especially for the cascaded inverter. However, this approach is limited to lower-level inverters, and its effectiveness may decrease with higher levels owing to increased complexity and control challenges [8]. Authors in [9] introduced a nine-level flying-capacitor inverter with reduced switches, capacitors, and gate drivers, aiming for a more power-efficient design verified through MATLAB/Simulink. Although the proposed topology simplified the circuit and lowered the cost, it suffered from a high THD of 18.13% and a large overall component count, which limits its practical efficiency and scalability. Authors in [10] studied a Single-Source Cascaded Multilevel Inverter (SCMLI) topology using an impedance network and a Self-voltage-Balancing Circuit (SBC) to achieve a 1.5× voltage boost with fewer switches and only one DC source. The proposed design effectively generated multiple output levels and improved the voltage balance. However, a large number of capacitors are required, increasing the overall component count. Furthermore, due to the increasing output voltage levels, the system complexity and control challenges also increased, which may limit the practical scalability of the system.

In this study, a novel design was developed for an MLI with a reduced component count. Various PWM techniques were applied to mitigate the harmonics and improve the overall output quality.

II. RESEARCH METHODOLOGY FOR THE HYBRID-ASYMMETRIC MLI

Figure 1 depicts the generalized structure of the proposed topology. To increase the output voltage levels, reduce the THD, and improve the power quality, an H-bridge extended by a single-phase half-bridge inverter was designed. The proposed topology comprised eight unidirectional power switches (S_1-S_8) and three DC voltage sources (V_1, V_2, and V_3). The former is called a cascaded connection of a Developed H-Bridge and Half-Bridge inverter (DHB-HB-MLI). The nine levels were intended to be produced at the output by the basic unit of the proposed model. With a V_{DC} value of 12 V, the DC source magnitudes were chosen using a 2:2:1 ratio. The design equations, switching states, current routes, Maximum Blocking Voltage (MBV), and Total Standing Voltage (TSV) calculations using a reference output waveform served as the foundation for the MLI parameters. The latter were computed to estimate the hybrid MLI performance. Table I shows the states of the switches.

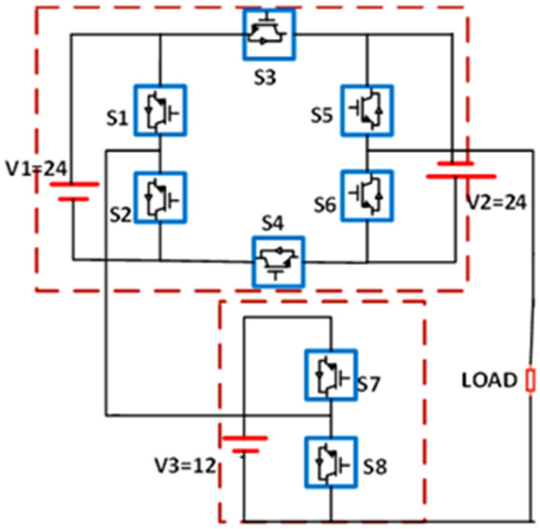


Fig. 1. Topology of the proposed hybrid asymmetric MLI.

The number of levels N_L required is given by:

$$N_L = 2n + 5 \quad (1)$$

where n is the total number of voltage sources in each leg.

The mathematical relationship for the number of switches N_{SW} needed is:

$$N_{SW} = 2n + 4 \quad (2)$$

The required gate driver circuits N_{GD} are provided using:

$$N_{GD} = 2n \quad (3)$$

The required number of DC sources is provided by:

$$N_{DC} = n + 1 \quad (4)$$

TABLE I. STATES OF SWITCHES FOR THE PROPOSED 9-LEVEL MLI

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output level
1	1	0	1	0	1	0	1	0	$+1V_{DC}$
2	0	1	1	0	1	0	0	1	$+2\ V_{DC}$
3	0	1	1	0	1	0	1	0	$+3\ V_{DC}$
4	0	1	1	0	0	1	0	1	$+4\ V_{DC}$
5	0	1	0	1	0	1	0	0	0 V
6	1	0	0	1	0	1	1	0	$-1\ V_{DC}$
7	1	0	0	1	0	1	0	1	$-2\ V_{DC}$
8	1	0	0	1	1	0	1	0	$-3\ V_{DC}$
9	1	0	0	1	1	0	0	1	$-4\ V_{DC}$

A. Switching Operation

The switching modes for the following 9-level are displayed in Figure 2, where in State 1, switches S_1, S_3, S_5, and S_7 are in the active state and generate a voltage of +1 V_{DC}. Similarly, in State 2, the switches S_2, S_3, S_5, and S_8 are in the active state and generate a voltage of +2 V_{DC}. In state 3, switches S_2, S_3, S_5, and S_7 are in the active state and generate a voltage of +3 V_{DC}. In state 4, switches S_2, S_3, S_6, and S_8 are in the active state and generate a voltage of +4 V_{DC}. The operation of the negative cycle is portrayed in Figure 2.

B. TSV Calculations

Technoeconomic analyses of MLI have shown that the TSV of the switches is a critical factor. TSV refers to the MBV a switch must withstand in the off state. Reducing this voltage stress lowers the cost of the inverter [11]. For example, in State 1 (Figure 2), switches S_1, S_3, S_5, and S_7 are on, producing +1 V_{DC} across the load, whereas switches S_2 and S_4 experience the highest voltage stress of 1 V_{DC}. Table II summarizes the MBVs for all switches in the proposed 9-level hybrid asymmetric MLI:

$$MBV_{s1} = MBV_{s2} = 2V_{DC} \quad (5)$$

$$MBV_{s5} = MBV_{s6} = 2V_{DC} \quad (6)$$

$$MBV_{s3} = MBV_{s4} = 4V_{DC} \quad (7)$$

$$MBV_{s7} = MBV_{s8} = 1V_{DC} \quad (8)$$

The TSV is calculated using:

$$TSV = \sum_0^1 MBV_{sin} \quad (9)$$

$$TSV = MBV_{s1} + MBV_{s2} + \cdots + MBV_{s8} \quad (10)$$

$$TSV = 2V_{DC} + 2V_{DC} + 4V_{DC} + 4V_{DC} + 2V_{DC} + 2V_{DC} + 1V_{DC} + 1V_{DC} \quad (11)$$

$$TSV = 18V_{DC} \quad (12)$$

The TSV per unit can be estimated using:

$$TSV_{PU} = \frac{V_{TSV}}{V_{0max}} = 4 \quad (13)$$

where V_{TSV} denotes the value of TSV and V_{omax} is the maximum output voltage: $V_{omax} = 2nV_{DC} = 4V_{DC}$. The value of TSV per unit for the 9-level MLI is calculated by:

$$TSV_{PU} = 4$$

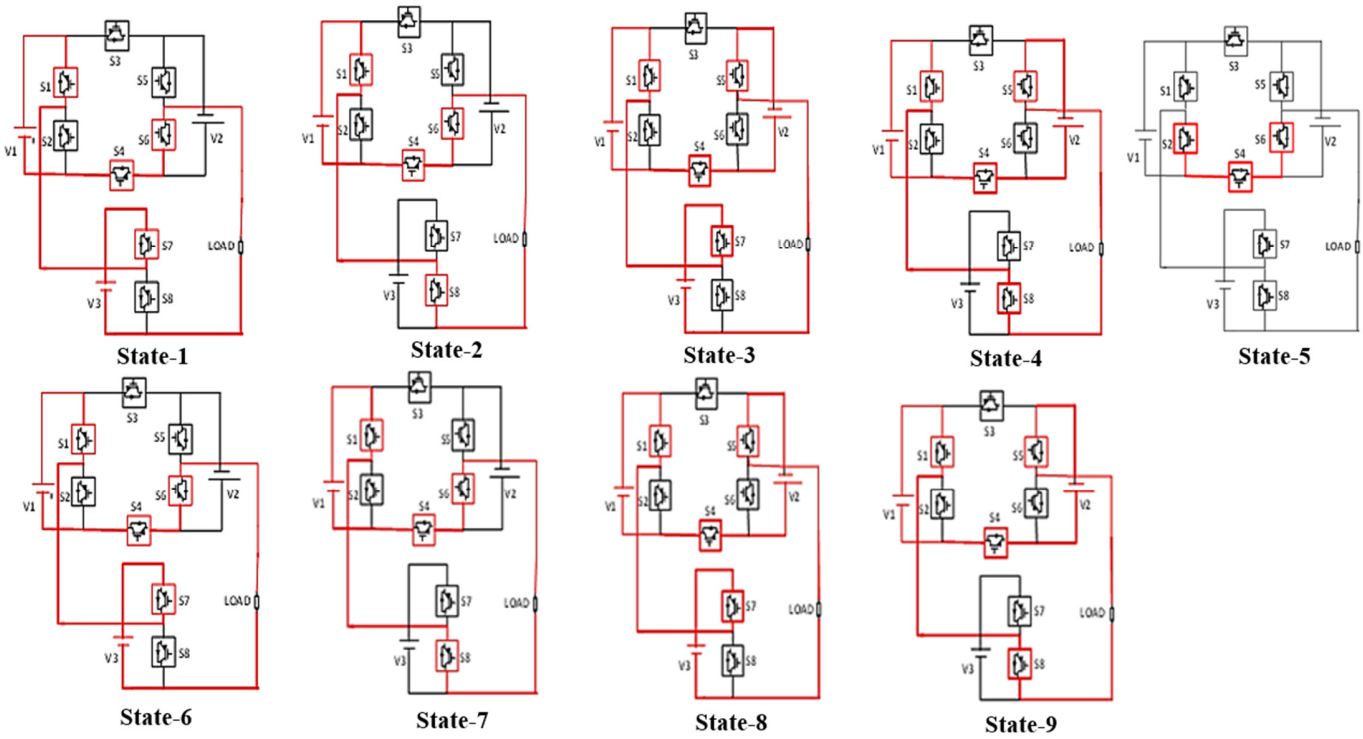


Fig. 2. Switching operation of the hybrid asymmetric MLI: State-1(+1), State-2(+2), State-3(+3) State-4(+4V), State-5(0), State-6(-1), State-7(-2), State -8(-3), State-9 (-4).

TABLE II. MBV ACROSS 9-LEVEL HYBRID ASYMMETRICAL MLL

State	Active sources	Stress switches	Max stress across switches	Output
1	V_3	S_8	S_8	1 V
2	V_1	S_1, S_4	S_1, S_4	2 V
3	V_1+V_3	S_1, S_4, S_8	S_1, S_4	3 V
4	V_1+V_2	S_1, S_4, S_5	S_4	4 V
5	-	-	-	0 V
6	-(V_1+$V3$)	S_2, S_3, S_8	S_3	-1 V
7	-(V_1)	S_2, S_3	S_3	-2 V
8	-(V_1+V_2-V_3)	S_2, S_3, S_6, S_8	S_3	-3 V
9	-(V_1+V_2)	S_2, S_3, S_6	S_3	-4 V

C. Cost Function for the Hybrid Asymmetric MLI

The Cost Function (*CF*) is a mathematical expression used to evaluate the performance of the MLI. The *CF* of an asymmetric MLI is provided by:

$$CF = (N_{sw} + N_{gd} + N_D + N_C + \propto TSV_{PU}) \times N_{DC} \quad (14)$$

The cost function is denoted by *CF*, the capacitors by N_C, the diodes by N_D, and α denotes the weight coefficient.

The value of the weight coefficient (α) is always more than 1 (1.5) and less than 1 (0.5). The *CF* per Level (*CF/L*) for a 9-level asymmetrical MLI is calculated as:

For α = 0.5: *CF/L* = 14 × 3/9 = 4.75

For α = 0.5: *CF/L* = 18 × 3/9 = 6.25

D. Calculation of Component Count per Level

The total sum of the active and passive components divided by the number of levels is defined as the Components Count per Level (*CC/L*). *CC/L* can be determined using:

$$\frac{CC}{L} = \frac{N_X+N_{SW}+N_C+N_D+N_{DC}+N_T}{N_L} \quad (15)$$

where the number of transformers is denoted by N_T, and the number of other components is denoted by N_X. The nine-level MLI had a CC/L ratio of 1.67.

E. Multicarrier PWM

MLIs use various PWM-based multicarrier modulation techniques, such as PS-PWM, LS-PWM, and SVPWM, to reduce THD and improve the output quality. These methods utilize (N_L-1) carrier signals, where N_L is the number of output voltage levels with identical frequency and amplitude and a centered reference waveform. PWM enables simple voltage regulation, reduces lower-order harmonics, minimizes filtering requirements, lowers power consumption, and allows digital control [11]. In the proposed DH-CHB-MLI design, LS-PWM with eight carriers and one reference signal were used to generate the switching states. LS-PWM has three types: PD, POD, and APOD. The general PWM control scheme is illustrated in Figure 3.

F. Phase Disposition

Figure 4 illustrates the PD PWM technique applied to a 9-level MLI, where eight carrier signals are aligned in phase and a single sinusoidal reference signal is used. The reference is compared with all carriers to generate switching pulses that control the inverter output.

G. Phase Opposition Disposition

In this PWM technique, the carrier waves are 180◦ out of phase below the zero reference and in phase above it for the POD approach, as displayed in Figure 5.

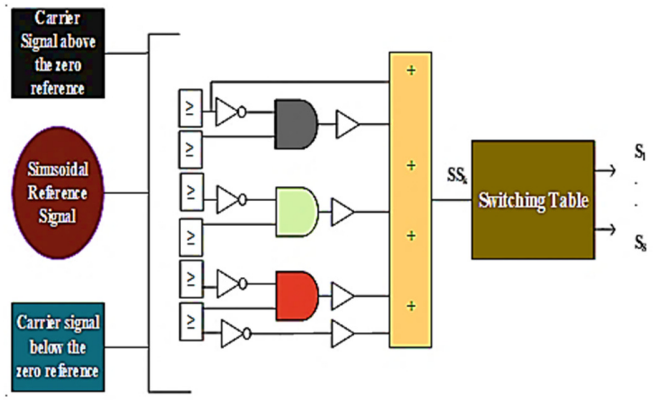


Fig. 3. PWM control scheme.

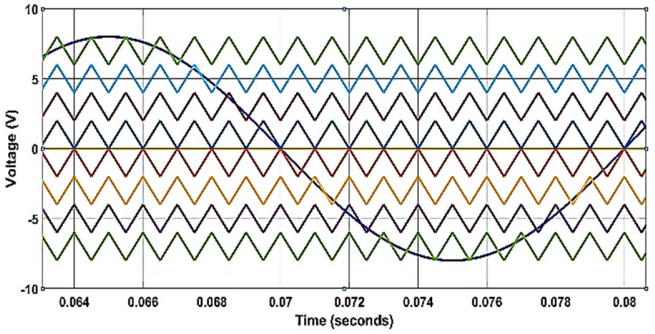


Fig. 4. PD type PWM technique.

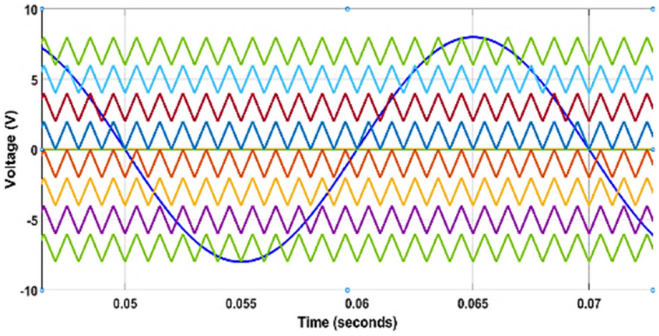


Fig. 5. POD type PWM technique.

H. Alternative Phase Opposition Disposition

For an N_L inverter, APOD involves a phase displacement of 180◦ in turns for each of (N_L − 1) carrier waveforms. The APOD is shown in Figure 6, demonstrating the carrier and fundamental waveforms. This technique involves phase displacement.

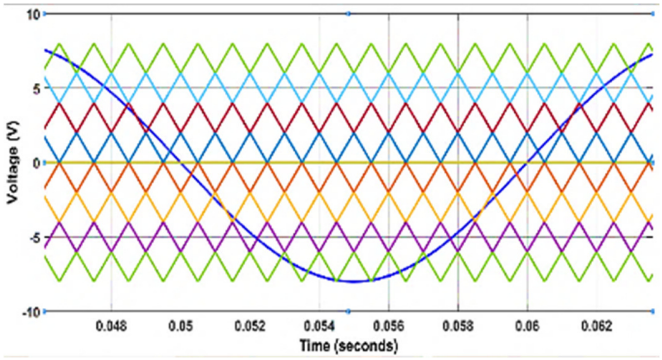


Fig. 6. APOD type PWM technique.

III. MATLAB SIMULINK MODELS

A. *Simulink Model of a PV System with DC-DC Boost Converter*

The Simulink model of a PV system with a DC-DC boost converter is presented in Figure 7 and its parameters are listed in Table III. The simulation involved varying the irradiance while keeping PV temperature constant. The boost converter increased the PV output voltage, regulated by a Maximum Power Point Tracking (MPPT) controller to maximize power extraction and maintain voltage stability under changing conditions. A scope monitored real-time DC output voltage. The controller also maintained a specific switching frequency to minimize harmonics and ensure efficient operation.

B. *Simulink Model of PV System with a Hybrid Asymmetrical MLI*

The hybrid MLI Simulink model is shown in Figure 8. MATLAB software was used to simulate this model. Eight Insulated Gate Bipolar Transistors (IGBT) switches and three DC sources were linked to create a hybrid MLI. In hybrid MLI, the multicarrier PWM technique's control circuit is used. The gating signal is sent to the switches utilizing a multicarrier PWM control circuit. These are employed to lower the MLI's harmonics. Table IV lists the parameters of the proposed hybrid MLI.

TABLE III. SIMULINK PARAMETERS OF PV SYSTEM WITH DC-DC BOOST CONVERTER

Parameter	Value
Voltage at MPPT (V_{mp})	4 V
Output circuit voltage (V_{oc})	6 V
No of series connected models per string	1 for 12 V, 2 for 24 V
Current at MPPT (I_{mp})	7.5 A
No. of parallel strings	2
Boost converter	
Inductance	$9.2\ 10^{-4}$ H
Capacitance	$46\ 10^{-6}$ F
DC boost voltages	12 V, 6 V

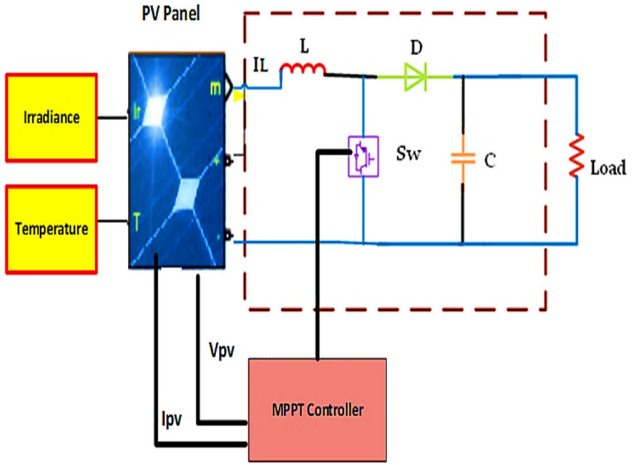


Fig. 7. Simulink model of a PV system with a DC-DC boost converter.

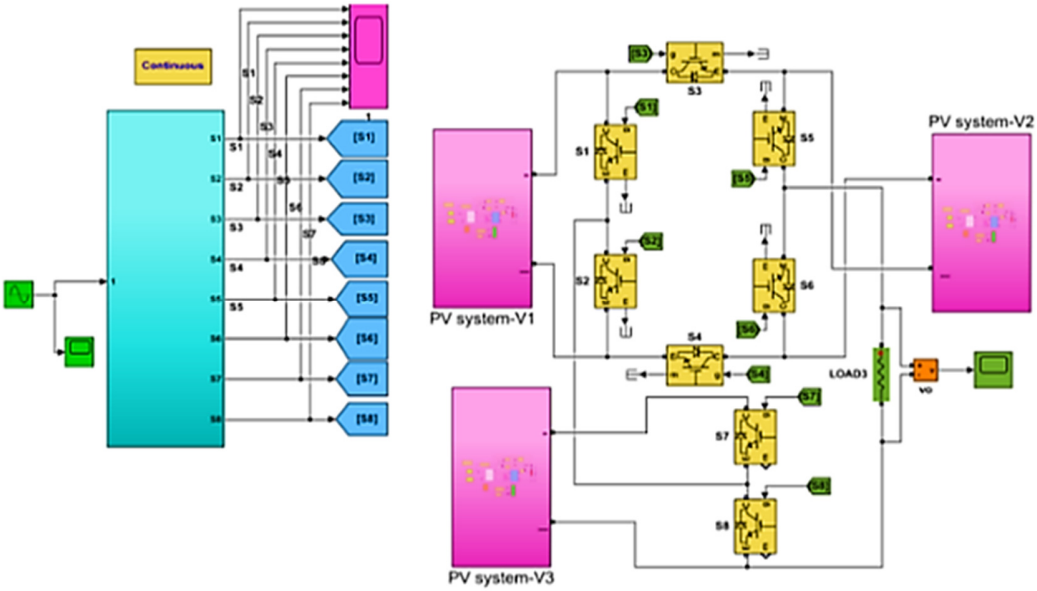


Fig. 8. Simulink model of hybrid MLI with a PV system.

TABLE IV. SIMULINK PARAMETERS OF HYBRID PV SYSTEM

Parameter	Value
No. of carrier signals	8
No. of DC voltage sources	3
Switch type	IGBT
No of switches	8
Frequency of reference signal	50 Hz
Switching frequency	1 kHz
Voltage magnitude	V_1=24 V, V_2=24 V, V_3=12 V

IV. RESULTS

A. Simulation Results of a PV System with DC-DC Boost Converter

Figure 9 illustrates the simulation results for the PV system equipped with a DC-DC boost converter. As shown in Figure 9(a), the irradiance was 800 W/m^2 for the first 0.1 s and then increased to 1000 W/m^2 for a duration of 0.1 s. After 0.2 s, the irradiance decreased to 900 W/m^2 for a duration of 0.1 s. Figure 9(b) demonstrates that the DC voltage was maintained at 12 V due to the MPPT controller. Similarly, Figure 9(c) shows the approximately constant voltage of 24 V.

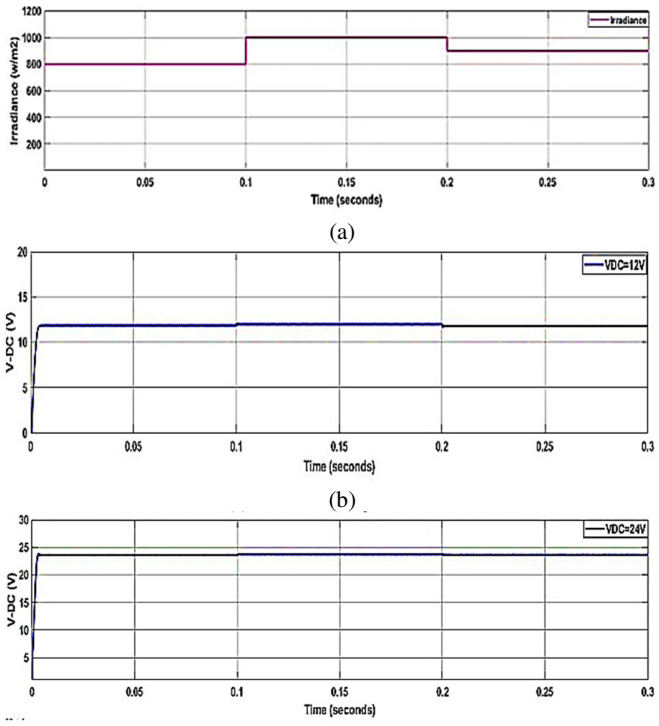


Fig. 9. Simulation results of a PV system with DC-DC boost converter: (a) PV irradiance, (b) boost converter voltage of 12 V, (c) boost converter voltage of 24 V.

B. Simulation Results of the Proposed Model Using Various PWM Methods

PD, POD, and APOD are carrier-based modulation methods for evaluating the proposed asymmetric hybrid 9-level MLI. The MLI used asymmetrical DC sources (V_1 = 12 V, V_2 = 12 V, V_3 = 6 V) and was tested with a 10 Ω resistive load. In the PD-PWM method, with a 1 kHz carrier frequency and 0.95 modulation index, a maximum RMS output voltage of 33.82 V was achieved.

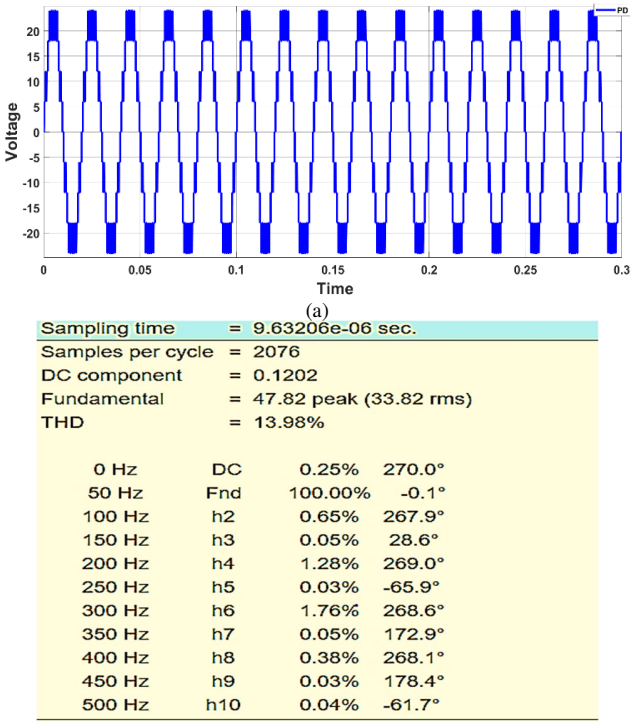
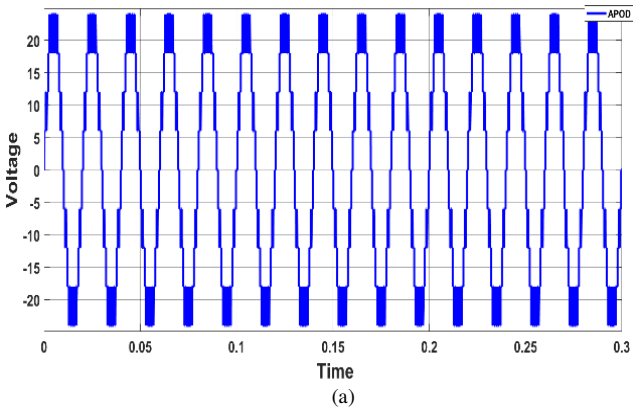


Fig. 10. PD results: (a) Output voltage, (b) THD % and odd harmonic values.

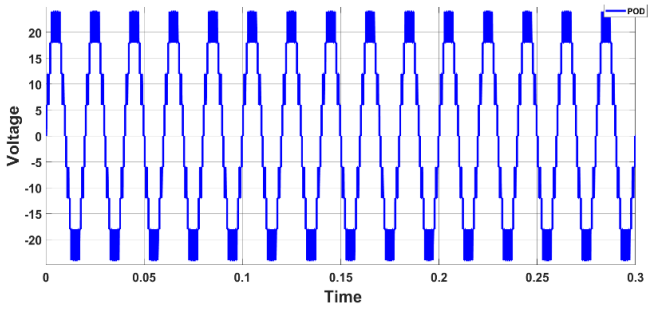
Figure 11(a) portrays the output voltage waveform of the nine-level MLI using the POD PWM method, with a constant carrier frequency and modulation index, yielding an RMS voltage of 33.83 V and 16.25% THD. Figure 13 highlights the 3rd, 5th, and 7th harmonics. A similar nine-level output was achieved using the APOD technique, with the THD analysis presented in Figure 12.



Sampling time	= 9.55231e-06 sec.		
Samples per cycle	= 2094		
DC component	= 0.01159		
Fundamental	= 47.84 peak (33.83 rms)		
THD	= 16.25%		
0 Hz	DC	0.02%	90.0°
50 Hz	Fnd	100.00%	-0.0°
100 Hz	h2	0.07%	129.5°
150 Hz	h3	0.30%	-1.9°
200 Hz	h4	0.05%	94.9°
250 Hz	h5	0.13%	184.8°
300 Hz	h6	0.02%	13.8°
350 Hz	h7	1.57%	180.4°
400 Hz	h8	0.04%	259.5°
450 Hz	h9	1.05%	181.0°
500 Hz	h10	0.01%	264.3°

(b)

Fig. 11. POD results: (a) output voltage and (b) THD% and odd harmonic values.



(a)

Sampling time	= 9.60246e-06 sec.		
Samples per cycle	= 2083		
DC component	= 0.001205		
Fundamental	= 47.81 peak (33.81 rms)		
THD	= 14.31%		
0 Hz	DC	0.00%	90.0°
50 Hz	Fnd	100.00%	0.0°
100 Hz	h2	0.06%	264.4°
150 Hz	h3	0.14%	-11.0°
200 Hz	h4	0.03%	185.0°
250 Hz	h5	0.80%	1.5°
300 Hz	h6	0.06%	189.9°
350 Hz	h7	2.51%	-0.5°
400 Hz	h8	0.08%	61.7°
450 Hz	h9	4.52%	0.9°
500 Hz	h10	0.06%	76.5°

(b)

Fig. 12. APOD results: (a) output voltage and (b) THD% and odd harmonic values.

The output voltage THD in the APOD technique was 14.31%, which is comparable to that of the PD technique and lower than that of the POD. Figure 13 displays the 3rd, 5th, and 7th harmonics. Table V compares the THD% across the three PWM strategies for both the R and RL loads and odd harmonics. PD achieved the lowest THD and odd harmonics (h3, h5, h7, and h9). APOD was worse than PD but exhibited better performance than POD in terms of THD and harmonic reduction. Overall, PD was the most effective PWM method for minimizing the THD and harmonics in the proposed MLI design.

TABLE V. COMPARISON OF THE DIFFERENT PWM PERFORMANCE FOR THE PROPOSED MLI

PWM technique	THD%	Odd harmonics % at R=10 Ω	THD%	Odd harmonics % at R=10 Ω and L=3 mH
PD	13.98%	h3 =0.05%, h5= 0.03%, h7=0.05%, h9=0.03%	14.05%	h3 =0.02%, h5= 0.01%, h7=0.05%, h9=0.03%
POD	16.25%	h3 =0.17%, h5= 0.89%, h7=2.51%, h9=4.52%	16.28%	h3 =0.35%, h5= 0.17%, h7=0.1.56%, h9=1.09%
APOD	14.31%	h3=0.14%, h5=0.80%,h7=2.51%. h9=4.52%	14.36%	h3 =0.16%, h5= 0.76%, h7=2.54%, h9=4.55%

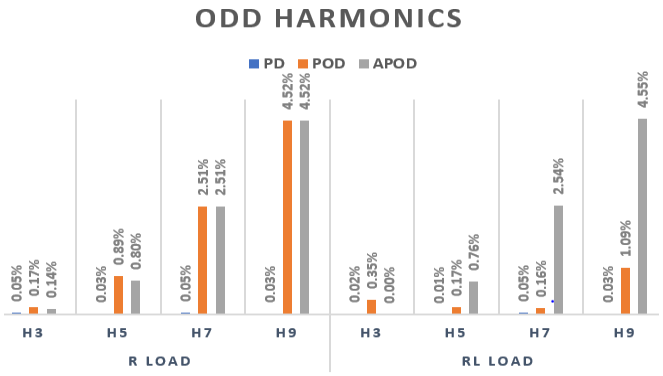


Fig. 13. Odd harmonics of PWM techniques with R and RL loads.

C. Comparison with Literature

To highlight the advantages of the proposed MLI topology, which is implemented with reduced components, a comparison with recent MLI designs is presented in Table VI and Figure 14. The parameters compared include the output levels, switches, capacitors, diodes, gate drivers, and DC sources.

TABLE VI. COMPARISON OF THE PROPOSED TOPOLOGY WITH OTHERS

Components	CHBMLI	DCMLI	FCMLI	SCMLI	Proposed MLI
No of sources	3	1	1	1	3
No of switches	8	8	9	7	8
Capacitors	0	3	2	5	0
Diodes	0	4	1	0	0
Levels	9	9	9	9	9
Drivers	5	6	10	3	4
References	[8]	[9]	[9]	[10]	

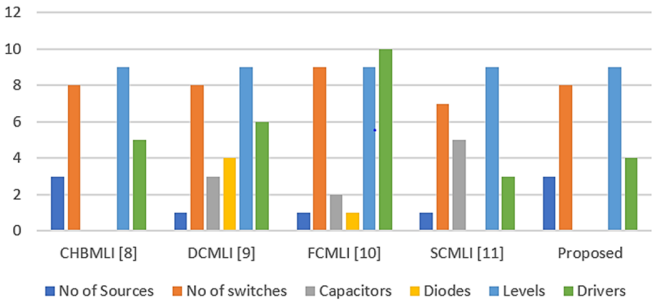


Fig. 14. Comparison of the total component implementation between the proposed topology and recent studies.

V. CONCLUSIONS

This study introduces a novel type of hybrid Multi-Level Inverter (MLI) called the Developed H-Bridge–Half-Bridge (DHB–HB), designed to improve the performance of photovoltaic systems. The proposed topology combines H-bridge and half-bridge circuits and uses three unequal DC voltage sources to produce a nine-level output voltage. This topology requires fewer switches and gate drivers, which reduces the cost and facilitates implementation and control. A DC-DC boost converter used an MPPT algorithm to maintain a stable voltage under variable irradiance. The design was simulated using MATLAB software. Among the three different Pulsed Width Modulation (PWM) techniques studied, the Phase Disposition (PD) technique exhibited the lowest Total Harmonic distortion (THD) of 13.98% and lower odd harmonics, which comply with the IEEE standards. Although POD and APOD reduced the unwanted odd harmonics, these methods demonstrated a slightly higher THD% of 16.25% and 14.31%, respectively. The proposed design also showed good performance analysis parameters, such as voltage stress, cost function, and number of components, compared to previous designs. The simple structure, low cost, and reliable operation make the proposed DHB-HB MLI suitable for future solar systems, grid-tied inverters, and other applications.

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