# A Frequency Multiplier Based on Time Recursive Processing

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*Abstract*—**This paper describes a digital frequency multiplier for a pulse rate. The multiplier is based on the recursive processing of the input and output periods and their time differences. Special emphasis is devoted to the techniques which provide the development of multipliers based on this principle. The circuit is defined by two system parameters. One is the ratio of two clock frequencies and the other is a division factor of a binary counter. The realization of the circuit is described. The region of the system parameters for the stable circuit is presented. The different aspects of applications and limitations in realization of the circuit are considered. All mathematical analyses are made using a Z transform approach. It is shown that the circuit can be also used in tracking and prediction applications. Computer simulations are performed to prove the correctness of the math and the whole approach.**

***Keywords-frequency multiplier; digital circuit; PLL; FLL***

## I. INTRODUCTION

The Time Recursive Processing (TRP) approach is based on the measurement and processing of the input and output periods and the time differences between them. As stated in [1-10], this approach is suitable for the development of different kinds of TRP Phase Locked Loops (TRP PLL) and TRP Frequency Locked Loops (TRP FLL), which possess some new additional properties in comparison to the classic PLL and FLL. Due to these new properties, the development of new kinds of circuits and applications is provided. The classic PLL and FLL might be roughly divided into analog, hybrid and digital ones. All of them are frequency based systems, their frequency and phase are physically interconnected with time. Due to this close interdependence, new kind of TRP circuits can be described using the period instead of the frequency and changing the phase by the time difference between the input and output signals. In order to describe TRP circuits, recursive equations, in form of linear discrete system, are used, providing a new approach to description, analysis, realization and applications. Unlike the classic PLL, which generates the output signal always in phase with the input signal, TRP PLL is able to provide very precise control time and phase shifting [1]. Power time shifters are further described in [2, 3]. The technique used for the realization of TRP PLL and TRP FLL is applied for the realization of frequency synthesizers in [4]. The applications of TRP PLL and TRP FLL for noise rejection are described in [5-7]. A wide range of tracking and prediction applications is described in [5, 6, 8]. Most of the algorithms described in [1-10] are suitable for usage in a software form. All electronics TRP applications can be realized in a software form that can be applied anywhere. All that is necessary is to determine the corresponding analogy between TRP electronics variables and the corresponding ones, relating to another field. Such a software predictor is described in [9]. Very complex systems, consisting of a lot of subsystems, can also function as a FLL, whose realization is based on the same TRP technique [10]. It is well known that a frequency multiplier can be realized by classic PLL or FLL, just by using a counter in a feedback connection. The factor of frequency multiplication, in such solutions, is equal to the division factor of the counter. In this article the mentioned principle of the frequency multiplication is applied to one suitable TRP PLL model. The analysis specifics in the realization and application of this approach are presented. The results obtained can be applied to any type of TRP PLL or TRP FLL.

## II. MATHEMATICAL DESCRIPTION OF THE CIRCUIT

One general case of the time relation between an input signal Sin and an output signal Sop of the circuit is shown in Figure 1. The periods $TI_0$, $TI_1$,….$TI_k$, $TI_{k+1}$, and $TO_0$, $TO_1$,….$TO_k$, $TO_{k+1}$, as well as the time differences $\tau_0$, $\tau_1$, $\tau_2$…..$\tau_k$, $\tau_{k+1}$, occur at discrete times respectively $t_0$, $t_1$, $t_2$,…..$t_k$, $t_{k+1}$. The discrete times $t_0$, $t_1$, $t_2$,….$t_k$, $t_{k+1}$ are defined by the falling edges of the pulses of Sop in Figure 1. Note that, unlike the classic PLL, all variables are distributed in time in Figure 1. The natural recursive relation (1), between the variables, yields from Figure 1. It was supposed that the time difference $\tau$ is positive if the input signal leads the output signal. Correspondingly, in case that the output signal leads, time difference $\tau$ will take the negative value through the analysis. Let us start analyzing the main algorithm of the circuit which is presented by (2), where m and q are the system parameters. We will see later on that the part $TO_{k+1}=TI_k+m\tau_{k+1}$ of (2) represents TRP PLL for its self. If TRP PLL is in the stable state, the output TO is equal to the input TI. The parameter q in (2) represents the division factor, which can be, generally, less or greater than one. The idea is to generate the output

period/frequency which is q times less/greater, so that after division by q, the circuit generates the output period which is equal to the input period. It is expected, guided by the known principles in the realization of the frequency multipliers by the conventional PLL, that the period/frequency before the division should be q times less/greater than the input period/frequency. However, the circuit does not behave according to the expectations. The following analysis will discover the proper functioning way of the circuit, described by (2), as well as the techniques which will enable the circuit to function as a frequency multiplier.

$$\tau_{k+1} = \tau_k + TI_k - TO_k \tag{1}$$

$$TO_{k+1} = \frac{TI_k + m \cdot \tau_{k+1}}{q} \tag{2}$$

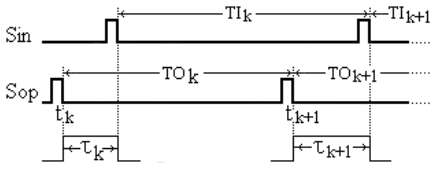


Fig. 1. Time relations between all variables of the circuit

According to (1) and (2), the circuit has two output variables, which depend on $TI_k$. The output variables are $\tau(k+1)=f[TI(k)]$ and $TO(k+1)=f[TI(k)]$. Note that, because of simplicity, TO(k), TI(k) and τ(k) are denoted in the article as $TO_k$, $TI_k$ and $\tau_k$. It is now necessary to find out the Z transform of the output variables τ(k+1) and TO(k+1) in order to analyze the properties of the circuit described. The Z transform of (1) and (2) are given by (3) and (4) respectively. Time constants $TO_0$ and $\tau_0$ are the initial values of the output variables TO(k) and τ(k), which appear at discrete time $t_0 = 0$.

$$z \cdot \tau(z) - z \cdot \tau_0 = \tau(z) + TI(z) - TO(z) \tag{3}$$

$$zTO(z) - zTO_0 = \frac{TI(z) + \left[z\tau(z) - z\tau_0\right] \cdot m}{q} \tag{4}$$

Calculating τ(z) from (3) and changing it into (4), it can be found out:

$$TO(z) = TI(z)\frac{z(\frac{m}{q} + \frac{1}{q}) - \frac{1}{q}}{z(z-1+m/q)} + \frac{TO_0 z(z-1) + \tau_0 z\frac{m}{q}}{z(z-1+m/q)} \tag{5}$$

In the same way, changing TO(z) from (5) to (3), can be calculated:

$$\tau(z) = TI(z)\frac{z-1/q}{z(z-1+m/q)} + \frac{-TO_0 \cdot z + \tau_0 \cdot (z+m/q)}{z(z-1+m/q)} \tag{6}$$

Two transfer functions, presented by (7) and (8), describe the output variables of the circuit in dependence on the input period. They are defined from (5) and (6) respectively.

$$H_{TO}(z) = \frac{TO(z)}{TI(z)} = \frac{z(m/q + 1/q) - 1/q}{z(z-1+m/q)} \tag{7}$$

$$H_\tau(z) = \frac{\tau(z)}{TI(z)} = \frac{z-1/q}{z(z-1+m/q)} \tag{8}$$

Step analysis will discover the properties of the circuit described. Let us suppose that the step function, TI(k)=TI=const., is applied to the input. If we change the Z transforms TI(z)=TI·z/(z-1) into (5) and (6), we will get the Z transform of the output variables for this input. Changing TI(z) into (5) and using the final value theorem, it is possible to find the final value of the output period in the time domain as $TO_\infty = \lim[TO(k)]$ if $k \to \infty$, using TO(z), as shown in (9). Applying (9), $TO_\infty$ is calculated and shown in (10). To complete the information about the system properties, it is necessary to determine $\tau_\infty$, i.e. the final value of τ(k). If TI(z) are substituted into (6), using the final value theorem in the same way like for $TO_\infty$, $\tau_\infty$ can be determined using (11). Applying (11), $\tau_\infty$ is calculated and shown in (12).

$$TO_\infty = \lim[(z-1) \cdot TO(z)]_{z \to 1} \tag{9}$$

$$TO_\infty = \lim[TO(k)]_{k \to \infty} = TI \tag{10}$$

$$\tau_\infty = \lim \tau(k)_{k \to \infty} = \lim[(z-1) \cdot \tau(z)]_{z \to 1} \tag{11}$$

$$\tau_\infty = TI \cdot (q-1)/m \tag{12}$$

The expressions (10) and (12) are valued only if the circuit is the stable system i.e. if $|z_1|<1$ and $|z_2|<1$, where $z_1$ and $z_2$ are the poles of the transfer function $H_{TO}(z)$ or $H\tau(z)$, given by (7) and (8). Since $z_1=0$, and $z_2 = 1-m/q$, it yields that the circuit is the stable system if (13) is satisfied. According to (10) and (12), it follows that the described circuit possesses the properties of a PLL. This conclusion comes out from the facts that the output period $TO_\infty$, for the stable system, equalizes the input period and that the time difference $\tau_\infty$ does not depend on the initial conditions $\tau_0$ and $TO_0$.

$$0 < m < 2q \tag{13}$$

## III. REALIZATION OF THE MULTIPLIER

Looking at (10), we can notice that regardless of the counter in feedback connection, the output period $TO_\infty$ is equal to the input period TI if the circuit reaches the stable state. The expected frequency multiplication is not performed, because the main algorithm, given by (2), compensated the influence of the division factor q to the output period $TO_\infty$. However, the influence of q is made on the final value of time difference $\tau_\infty$, see (12), and on the region of the parameter m in (13). Due to this influence, the region of m, for the stable system is enlarged. The region of the parameter for the stable system, according to (13), is presented in Figure 2.

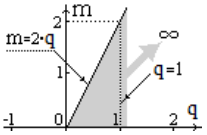


Fig. 2. The circuit is stable for the shaded region of parameters m and q. The circuit functions as a classic PLL for q=1.

Note that, according to (12), if q=1 then $\tau_\infty = 0$. The circuit functions as classic PLL. If q=1, it means that there is no counter in feedback connection. Let us first consider the realization of the circuit for q=1. Changing q=1 and $m=f_m/f_c$ into (2), where $f_m$ and $f_c$ are the clock frequencies of clock signals $S_m$ and $S_c$, (2) turns into (14). According to (14), $\tau_{k+1}$ is measured by the clock period $t_m=1/f_m$, $TI_k$ is measured by the clock period $t_c=1/f_c$ and $TO_{k+1}$ is generated by the clock period $t_c=1/f_c$. The principal scheme of the circuit, corresponding to (14), is shown in Figure 3. The circuit consists of Recursive Calculation Module (RCM) and Programmable Period Generator (PPG). RCM calculates $TO_{k+1}$ and PPG generates the output period at the next step. The realization of RCM, according to (14), can be easily performed using the technique described in [1-10].

$$f_c \cdot TO_{k+1} = f_c \cdot TI_k + f_m \cdot \tau_{k+1} \quad (14)$$

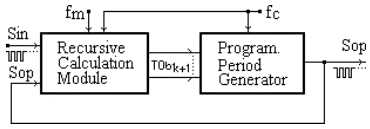


Fig. 3. The principal scheme of the circuit for q=1

PPG was described in details through [1-10], but in order to explain the development of the multiplier, it is now necessary to remember the general principles of its functioning. When the calculated $TO_{k+1}$ is entered as a binary word $TOb_{k+1}$ from RCM to PPG, PPG will count down pulses of clock signal $S_c$ as long as an up-down counter, incorporated in PPG, reaches zero. In that moment PPG generates the output pulse of $S_{op}$ which is, at the same time, used to enter the new binary word $TOb_{k+1}$, representing the next output period $TO_{k+1}$. After that, the described counting down, restarts and the process is continuously repeated. The result of this processing is the constant generation of pulses of $S_{op}$. The period of $S_{op}$ is $TO=TO_d \cdot t_c$, where $TO_d$ is the decimal value of $TO_b$.

Let us now suppose that the frequency of clock Sc is $q_c$ times greater. According to the previous explanation of the way of PPG functioning, it is obvious that the counting down would be $q_c$ times faster and the output period will be $q_c$ times decreased, because the new $TO=TO_d \cdot t_c/q_c$. In other words, we would get the output frequency, which is $q_c$ times greater than the input frequency. On the other hand, this would disrupt and destabilize an established mode of circuit functioning, because the expected output period which is fed into RCM, would be $q_c$ times decreased. To escape this disturbance at the input of RCM, it is necessary only to incorporate a counter in feedback connection whose division factor is $q_c$. At the output of the counter, the output period would be the expected one, just like in case of the circuit, shown in Figure 3, which corresponds to the case q=1. In other words, the influence of the increased clock frequency and the affect of the counter in feedback connection would compensate each other. In this way, the additional part of the circuit, outside of RCM, increases the output frequency $q_c$ times and immediately decreases it also $q_c$ times, providing the frequency multiplication of the input frequency by $q_c$, at the output of PPG. Due to fact that the additional part of circuit is outside of RCM, it does not obstruct the calculation in accordance with the main algorithm. It is now necessary to explain how it is possible to realize the described solution practically. The necessary additions, in comparison to the circuit presented in Figure 3, can be seen at the principle scheme of multiplier, shown in Figure 4. To realize the described principle of the frequency multiplication it is necessary to memorize the binary form of the current output period $TOb_k$ in a register "Reg". Binary form $TOb_k$ will be taken by PPG $q_c$ times during the calculation of the next output period $TOb_{k+1}$. Whenever PPG generates an output pulse of $Sop_q$, its trailing edge is differentiated. New generated pulse is fed to input "Load" of PPG over OR gate and it is used for the reentering of $TOb_k$ into PPG, providing the continuously generation of pulse rate $Sop_q$, whose frequency is $q_c$ times greater than an input frequency of Sin. After $q_c$ pulses of $Sop_q$ are generated, a trailing edge of $Sop_c$ will appear at the output of the counter. This trailing edge is differentiated and new generated pulse is used to preset the next binary form of the output period $TOb_{k+1}$ into register and into PPG, simultaneously. The binary word $TOb_{k+1}$ will be used to generate next $q_c$ pulses of $Sop_q$. Finally, in order to adapt $Sop_c$ to RCM, the pulses of $Sop_c$ are narrowed by monostable multivibrator MM. After the modification shown in Figure 4 is made, in comparison with the principal scheme shown in Figure 3, a new model of the principal scheme of the multiplier is shown in Figure 5. The modifications are made inside the PPG to compensate the effects of the counter in the feedback connection. Note that RCM modules in Figure 3 and in Figure 5 function completely in the same way, providing that the same input signal Sin is fed into them, so that most of the additional parts in Figure 4, together with the existing PPG, can be considered as a new expanded PPG (Ex-PPG), shown in Figure 5. Accordingly, signal Sop shown in Figure 3, is identical to signal Sop, shown in Figure 5.

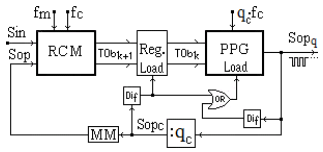


Fig. 4. The principal scheme of the multiplier. The multiplication factor is $q_c$.

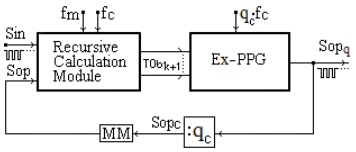


Fig. 5. The simplified principal scheme of the multiplier with Ex-PPG and a counter in the feedback connection. The multiplication factor is $q_c$.

One eight bit multiplier was realized with the standard integrated circuits for q=1 and m=1 ($f_m=f_c$). The multiplication factor, related to Ex-PPG, is $q_c=10$. The input period is the step function TI=1ms, corresponding to the frequency of 1kHz. The clock frequencies $f_c=f_m=30$ kHz, $q_c \cdot f_c=300$ kHz so that the ratio will be $TI/t_c=30$. The oscilloscope picture of the voltage waveforms, shown in Figure 6, was taken when the multiplier

was in the stable state. The chosen waveforms correspond to the signals Sin, $Sop_q$, $Sop_c$ and Sop, shown in Figure 5. In accordance with the chosen parameters, the multiplier functions as classic PLL, striving to reduce the time difference to zero. Due to the fact that TI/tc=30, the reduction is rather successful. The input and output periods are equaled and the time difference between the signals Sin and Sop is zero in Figure 6. However, at the output of Ex-PPG, signal $Sop_q$ is generated, whose frequency is 10kHz, i.e. it is ten times greater than the input frequency of 1kHz. The function of monostable multivibrator MM is also shown by signal Sop in Figure 6. Although the generation of the multiplied frequency was performed inside Ex-PPG, the generation of $Sop_q$ was controlled by the closed loop system and the multiplier possesses all properties of described TRP-PLL.

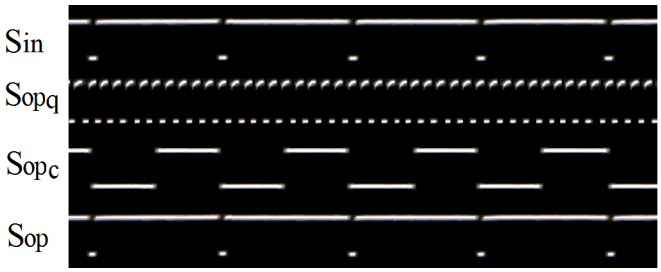


Fig. 6. The oscilloscope picture of the multiplier voltage waveforms for q=1, m=1 (fc=fm=30 kHz), $q_c$=10 and *TI*=1ms (frequency of 1kHz).

## IV. OTHER PROPERTIES OF THE CIRCUIT

Other circuit's properties are equally important either for the frequency multipliers or for other applications. To analyze them, it is necessary to simulate the functioning of the circuit for different practical situations. Besides the study of the new properties, the simulations are to enable better insight into the procedure and into the physical meaning of the variables described. At last, they are to prove the correctness of the previous analysis. All discrete values in simulations were merged to form continuous curves. All variables in the following diagrams were presented in time units, which can be, μsec, msec or any other, providing that the same time units are used for all time variables (TI, TO, and τ). It was more suitable to use just "time unit" or abbreviated "t.u." in the text and to omit the indication "t.u." in diagrams. All simulations were conducted in Matlab, using (1) and (2).

Let us first simulate the functioning of the circuit for the step input. The locking procedure of the circuit, for the step input, is considered for three cases in Figure 7. The step input is TI = 10 t.u. The parameters m and q are chosen carefully in order to demonstrate the properties of the circuit. All values of m and q, as well as the values of the initial conditions $TO_0$ and $\tau_0$ are presented in Figure 7. In Figure 7a can be seen that for any value of parameter m satisfying (13), the output period tends to the input period, but the transition time depends on the values of m and q. Note that if m=q (cases Nr. 1 and Nr. 2), the stable state is reached in two steps only. For all of three cases, the calculation of $\tau_\infty$ agrees with $\tau_\infty$ which can be seen on the simulated curves. According to (12), for case Nr. 1: $\tau_{1\infty}$=TI·(q-1)/m=10·(1-1)/1=0 t.u., for case Nr. 2: $\tau_{2\infty}$=TI·(q-1)/m=10·(2-1)/2=5 t.u. and for case Nr. 3: $\tau_{3\infty}$=TI·(q-1)/m=10·(6-1)/4.7=10.63 t.u. The same simulated results can be seen in Figure 7a. The agreement between the simulated and calculated values, confirms the correctness of the simulation results and the correctness of the whole approach. The merged discrete values for the case Nr. 1, representing the output variables $TO_1$ and $\tau_1$ in Figure 7a, are shown in the real time, in Figure 7b. This presentation is given in form of the pulse rates. It reveals the real time relations between all input and output variables and helps the better understanding of the physical mining of the simulated curves. All values, shown in Figure 7b, are taken from the simulation results, but they can be also calculated manually, step by step, using (1) and (2). According to the mathematical analysis and simulation results obtained, the circuit functions as classic PLL for m=1 and q=1. These parameter values were used for the development of the realized multiplier. However, the parameters can take any values satisfying (13).

It is of interest to investigate the ability of the circuit to track a ramp function (velocity function). To illustrate this ability, let us determine well known velocity error, providing that the input period is the ramp function $TI(k)=TI_V(k)=p\cdot k$, where p is a time constant. The definition of velocity error is $K_V=\lim[TO_V(k)-TI_V(k)]_{k\to\infty}$. The previous expression can be transform into $K_V=\lim\{TI_v(k)[H_{TO}(k)-1]\}_{k\to\infty}$, where $H_{TO}(k)$ is the inverse Z transform of the transfer function $H_{TO}(z)$, given by (7). Due to the final value theorem, it is possible to find Kv using another expression, given in Z transform form $K_V = \lim\{(z-1)\cdot TIv(z)\cdot[H_{TO}(z)-1]\}_{z\to1}$. Using the previous expression and Z transform of velocity function $TI_v(z)=Z(p\cdot k)=pz/(z-1)^2$, $K_V$ is calculated and presented by (15) according to which, the output of the circuit will track the velocity input without an error only if q=1. Otherwise the output will track the velocity input with the constant error $K_V$.

$$Kv = p\cdot(1-q)/m \qquad (15)$$

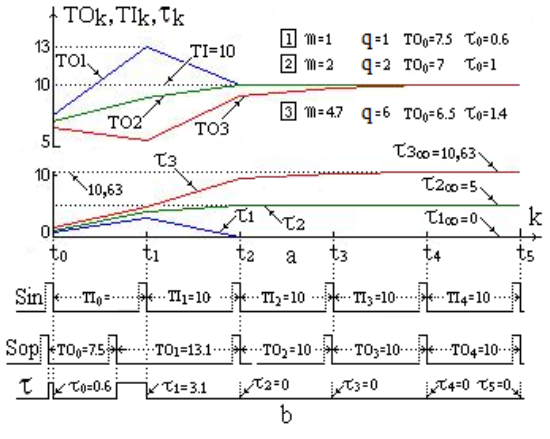


Fig. 7. (a). The output period tends to the input period and the final value of time difference $\tau_\infty$ = *TI*(q-1)/m. (b). All periods of Sin, Sop and time differences $\tau_k$, for the case Nr. 1, are calculated and presented to show the real time relation between variables. For this case, m=1 and q=1 ($\tau_\infty$=0) and the circuit functions as a classic PLL.

To complete the information about the system properties, it is necessary to determine $\tau_\infty$, i.e. the final value of $\tau(k)$ for q=1. If $TI(z)=TI_v(z)$ and q=1 are substituted into (6), we will get $\tau_v(z)$. Using the final value theorem, $\tau_{v\infty}$ is determined and shown by (16).

$$\tau_{V\infty} = \lim[(z-1)\tau_V(z)]_{z\to 1} = p/m \qquad (16)$$

To prove the correctness of the previous analysis, three cases of the locking procedure are simulated and presented in Figure 8 for the velocity input $TI_k=(10+2\cdot k)$ t.u., (p=2 t.u.). According to case Nr. 1 in Figure 8a, the circuit is able to track the velocity input without an error if q=1. For cases Nr. 2 and Nr. 3, q is not equal to one and the circuit tracks the velocity input with constant velocity errors. According to (15) the velocity errors could be calculated as $K_{v1}=p\cdot(1-q)/m=2\cdot(1-1)/1=0$ t.u., $K_{v2}=2\cdot(1-2)/2=-1$ t.u. and $K_{v3}=2\cdot(1-6)/4.7=-2.127$ t.u. The same values of $K_{v1}$, $K_{v2}$, and $K_{v3}$ were reached by simulation, which are presented in Figure 8c. The time differences for these three cases are shown in Figure 8b. For the case Nr. 1, q=1 and the final value $\tau_{v1\infty}$ can be calculated using (16). According to (16), $\tau_{v1\infty}=p/m=2/1=2$ t.u. The same value of $\tau_{v1\infty}$ was calculated by simulation in Figure 8b. For the cases Nr. 2 and Nr. 3, q is not equal to one and the time differences $\tau_{v2\infty}$ and $\tau_{v3\infty}$ tend to infinity. Regarding the obtained results, it is more suitable to choose q=1 for the realization of the multiplier. Firstly, the circuit possesses the better tracking properties. Secondly, in case that q is not equal to one, the requirements for the circuit capacity are stronger in the tracking applications, since the variable $\tau$ can reach undesirable large value. Another important conclusion is that the circuit is extremely fast if m=q. According to Figures 7 and 8, if q=m, the circuit takes only two steps to reach the stable state (cases Nr. 1 and Nr. 2).

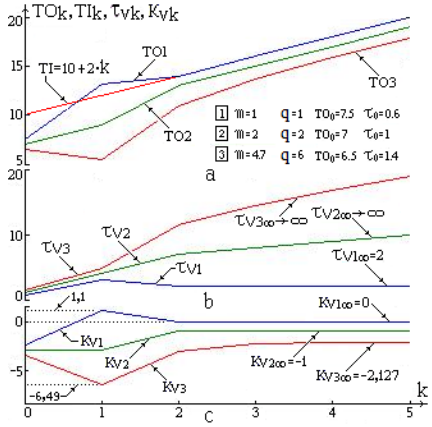


Fig. 8. The transition and stable state of the circuit for the velocity input: (a). The output periods track the input periods for three cases. (b). The corresponding time differences are presented. For the case Nr. 1 (q=1), according to (16), $\tau_{v1\infty}=p/m=2$. (c). The simulated velocity errors are in accordance with (15). For the case Nr. 1 (q=1), according to (15), $K_{v1\infty}=0$.

## V. CONCLUSION

The description, simulation and presentation of the realized multiplier demonstrate a new technique for a practical application of TRP circuits. This technique can be applied for the realization of frequency multipliers, as a type of upgrade, to any type of TRP PLL or TRP FLL. However, the described technique can also be used for frequency multiplication, independently of TRP circuits, even as an open loop system. The presented theoretical approach also provides a contribution to the field of the phase shifting based on TRP PLL. Some TRP PLL are able to provide different types of controlled phase shifting, either by using an outside control word or by using the system parameters. It was demonstrated in this paper that a division factor of a counter, positioned in a feedback connection in a TRP PLL, can also be used for phase shifting. As shown, the described circuit is suitable for tracking and prediction applications. The proposed circuit provides the capability to regulate the transition speed so that it can be adapted to specific application. The precision of the multiplication is limited by the capacity of the built-in up-down counters. Higher precision requires greater circuit capacity. The maximum factor of the frequency multiplication is limited by the speed of the used integrated circuits and by the required precision of the multiplication.

## REFERENCES

[1] D. M. Perisic, M. Bojovic, "Application of Time Recursive Processing for the Development of the Time/Phase Shifter", Engineering, Technology & Applied Science Research, Vol. 7, No. 3, pp. 1582-1587, 2017

[2] D. M. Perisic, M. Perisic, S. Rankov, "Phase Shifter Based on a Recursive Phase Locked Loop of the Second Order", Revue Roumaine des Sciences Techniques, Serie Electrotechnique et Energetique, Vol. 59, No. 4, pp. 391–400, 2014

[3] D. M. Perisic, A. Zoric, D. Babic, D. D. Perisic, "Recursive PLL of the First Order", Przeglad Elektrotechniczny, Vol. 89, No. 7, pp. 50-53, 2013

[4] D. M. Perisic, A. Zoric, S. Obradovic, D. D. Perisic, "FLL as digital period synthesizer based on Binary Rate Multiplier control", Przeglad Elektrotechniczny, Vol. 89, No. 1, pp. 145-148, 2013

[5] D. M. Perisic, M. Bojovic, "Multipurpose Time Recursive PLL", Revue Roumaine des Sciences Techniques, Serie Electrotechnique et Energetique, Vol. 61, No. 3, pp. 283–288, 2016

[6] D. M. Perisic, A. Zoric, M. Perisic, D. Mitic, "Analysis and Application of FLL based on the Processing of the Input and Output Periods", Automatika, Vol. 57, No. 1, pp. 230–238, 2016

[7] D. M. Perisic, M. Perisic, D. Mitic, M. Vasic "Time Recursive Frequency Locked Loop for the tracking applications", Revue Roumaine des Sciences Techniques, Serie Electrotechnique et Energetique, Vol. 60, No. 2, pp. 195–203, 2015

[8] D. M. Perisic, A. Zoric, M. Perisic, V. Arsenovic, Lj. lazic "Recursive PLL based on the Measurement and Processing of Time", Elektronika ir Elektrotechnika, Vol. 20, No. 5, pp. 33-36, 2014

[9] D. M. Perisic, A. Zoric, D. Babic, D. D. Perisic, "Decoding and Prediction of Energy state in Consumption control", Revue Roumaine des Sciences Techniques, Serie Electrotechnique et Energetique, Vol. 58, No. 3, pp. 263–272, 2013

[10] D. M. Perisic, A. Zoric, S. Obradovic, S. Spalevic, "Application of Frequency Locked Loop in Consumption Peak Load Control", Przeglad Elektrotechniczny, Electrical Review, Vol. 88, No. 1b, pp. 264-267, 2012

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