SRAM Design and Analysis Using TIGFET

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ABSTRACT

Continuous CMOS scaling can be enabled with nanowire transistor technologies such as the Three Independent Gate FET (TIGFET). TIGFET can further reduce the leakage current compared to FinFET, using Schottky barriers, increasing the speed of operation. As technology nodes become smaller, the number of Static Random Access Memory (SRAM) cells connected to a single word line grows, leading to an increase in coupling capacitance. With this, the power consumption of the SRAM increases, and the performance is degraded. A fundamental 6-T SRAM cell was developed utilizing TIGFET on a 10nm scale, and its performance was evaluated based on stability, leakage power, average power, and delay metrics. Write delays of 40 ns and read delays of 38.7 ns show better performance compared to a MOSFET-based design. The SNM values for TIGFET-SRAM were 0.36 V, 0.25 V, and 0.32 V in hold, write, and read modes, respectively, offering good stability. The design was simulated using the Synopsys HSPICE tool, and its results were compared with those of a MOSFET-SRAM cell.

Keywords-TIGFET; SRAM; high-performance; leakage power; static-noise-margin; reconfigurable devices

I. INTRODUCTION

For many years, the semiconductor industry has focused on scaling MOSFETs to develop System on Chip (SOC) technology by integrating a greater number of transistors onto a single Integrated Circuit (IC). The most attractive approach is to scale the supply voltage to optimize the system [1]. However, this results in a notable increase in delay, an increase in subthreshold leakage current, and a decrease in ON current when operating at lower supply voltages. The main approaches to transistor scaling and geometry optimization to increase functional density are slowly approaching physical limits [2]. To overcome the challenges faced by modern portable systems, engineers are focusing on alternative high-performance devices. Embedded SRAM is the most common type of memory for on-chip data storage and accounts for a large portion of power and area. In microprocessors, the cache occupies 70% of their total die area. Therefore, it is essential to focus on the optimization of SRAM circuits [3] using novel transistor technologies.

Leakage power consumption accounts for 30% to 50% of the total power consumption of a SOC, being a predominant factor [4]. Using FinFET technology at 22 nm improves electrostatic control and minimizes short-channel effects [5]. By improving the gate control, short channel effects due to continuous scaling down the device can be alleviated [6]. Multiple gate devices have been proposed to improve gate control [7]. FinFETs, also known a tri-gate FETs [8], have been used extensively to solve the difficulties of device scaling down to 22 nm technology. Computing-in-Memory (CiM) architectures have been developed for improved energy efficiency and increased DPA resiliency [9]. Negative capacitance FETs can be used in CiM cipher S-box with 8T-SRAM to achieve higher energy efficiency [10].

In FinFETs, the conducting channel is covered with dielectrics and gate materials on all three sides to achieve better electrostatic control and reduce leakage current. However, as size decreases, threshold voltage variation and mobility degradation are anticipated to increase significantly when scaling down FinFETs to below 10 nm. As a consequence of this phenomenon, innovative transistor paradigms enhance operational capabilities through the modification of their device attributes in real-time [11]. By utilizing polarity-controlled transistors [12], efficient designs can require fewer physical resources in the integrated circuit, thereby enhancing functionality while consuming less power. Using reconfigurable field-effect transistors, unipolar n-type and p-type transistors can be configured dynamically during runtime [13]. This results in a significant increase in functionality compared to traditional CMOS technology [14], where the physical properties and interconnection layout of each transistor define each logic cell. Additionally, the transistor count necessary for advanced circuit design can be significantly reduced with the same functionality, leading to energy efficiency, reduced chip area, and delay [15].

The leakage current can be effectively decreased by regulating the Schottky barriers. The vertically-stacked Three Independent-Gate SiNWFET (TIGFET) exhibits ambipolar behavior, within which both n-type and p-type device characteristics can be observed [16]. In [17], the history of RFET research was presented, from early device-level studies to the current focus on circuit and system-level applications. Advanced devices can be used for several applications to meet the current requirements of the semiconductor industry.

This paper presents the design of a 6-T SRAM cell using SiNW-TIGFET at 10 nm, analyzing its performance in terms of power dissipation and stability along with butterfly curves.

II. DEVICE DETAILS OF TIGFET

TIGFETs can be operated in different modes due to extra gate terminals. A p-type and n-type transistor can be derived from a single TIGFET by applying different electrical potentials to the side gates, and multiple threshold logic can also be implemented [18]. A TIGFET with a vertical stack of multiple nanowires decides the driving strength of the device without impacting its area, but at the expense of greater capacitance [19]. This device offers superior electrostatic control and scalability properties, allowing tuning of the threshold voltage. Configurable high- and low-V_t circuits can be achieved with different connection schemes for high performance and low leakage operation. In addition, the device can be integrated into existing CMOS manufacturing processes without requiring major changes.

Figure 1 shows the structure of the device with three independent gates: the Control-Gate (CG), the Polarity-Gate at the Source (PGS), and the Polarity-Gate at the Drain (PGD). Figure 2 shows a symbolic representation. The channel's potential barrier is controlled by CG, and the Schottky barriers at the source and drain are modulated by PGS and PGD. TIGFETs can be operated in different configurations with these three gates [20]. Figure 3 shows the voltage-current characteristics of TIGFET. TIGFET has two forms of switching mechanisms.

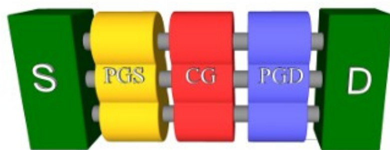

Fig. 1. Structure of TIGFET with vertically stacked SiNWs as a channel.

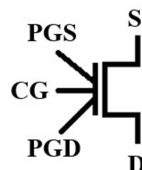

Fig. 2. Symbolic representation of TIGFET.

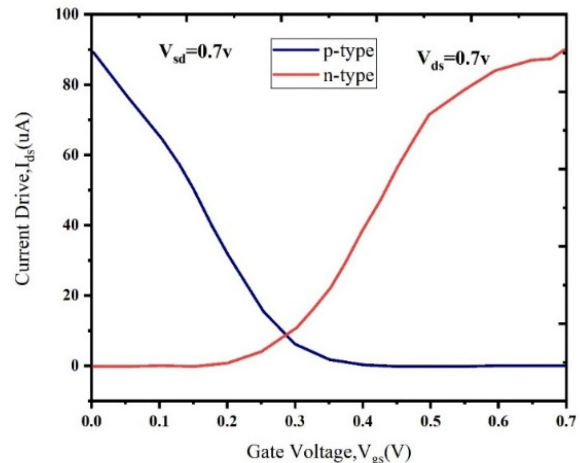

Fig. 3. Transfer characteristics of TIGFET [21]

The first one uses thermally assisted tunneling through Schottky barriers by the biasing voltages at PGS and PGD. The symmetrical $I-V$ characteristics of TIGFET, as shown in Figure 3, exhibit inherent resilience to side channel attacks. The maximum I_d that can be sourced from a TIGFET at a supply voltage of 0.7 V is 90.2 μA and 89.25 μA for n-type and p-type devices, respectively. The polarity gates PGS and PGD can independently modulate the thickness of Schottky barriers to force electrons and holes toward the channel, respectively. With this feature, TIGFETs can be used to implement high-performance designs with low leakage current. If there is a significant potential difference between the PGS and the source, the thin Schottky barriers allow electrons to enter the channel. Similarly, if there is a large potential difference between PGD and drain, the thin Schottky barrier allows the formation of a channel with holes. If the potential difference between the nodes PGS and Source and the PGD and Drain nodes is zero, no carriers will flow over the Schottky barriers, forcing the device to turn off. The second one is through the CG, which is similar to a MOSFET gate and forms a barrier at the center of the channel to regulate current flow. Table I shows the state of the device for different voltages. TIGFET can mimic an ordinary MOSFET by obtaining unipolar n-type and p-type transistors with the application of constant bias voltage to both the PGS and PGD polarity gates [22]. With this feature, a CMOS-style circuit design can be attained by replacing every MOSFET with the required TIGFET. Due to the presence of multiple gates, the circuit can be implemented with fewer gates [15]. This extra feature facilitates TIGFET technology, as two series n-type or p-type transistors can be merged, resulting in a single transistor, so that the number of transistors in the circuit design can be reduced [23].

TABLE I. GATE POTENTIALS FOR SEVERAL TIGFET CONFIGURATIONS

Type of device	Device condition	Applied potentials		
		V_{PGS}	V_{CG}	V_{PGD}
n-type	OFF	V_{dd}	0	V_{dd}
	ON	V_{dd}	V_{dd}	V_{dd}
p-type	OFF	0	V_{dd}	0
	ON	0	0	0

A basic inverter was designed using TIGFET and simulated at varied operating voltages from 0 to 1 V with a step of 0.1, shown in Figure 4(b). From this Voltage Transfer Characteristic (VTC), as the gate voltage increases, the output drive current also increases, which is similar to a MOSFET.

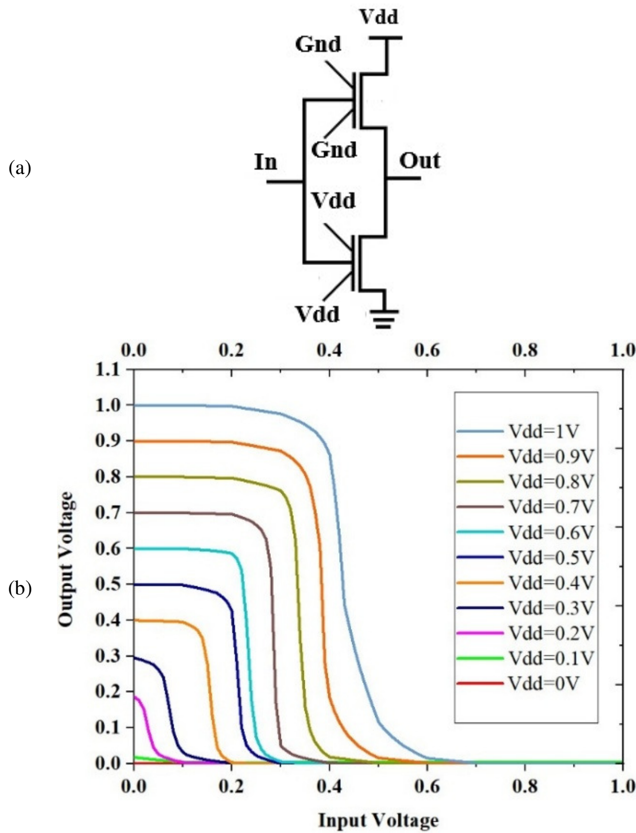

Fig. 4. (a) Schematic diagram of the inverter using TIGFET, (b) VTC characteristic of the basic inverter at varied potentials.

III. DESIGN OF SRAM USING TIGFET

Figure 5 shows the basic 6-T SRAM cell using MOSFET. This is a cross-coupled inverter along with access transistors, which can be operated in write mode, to write the data from the bit-lines BL and BLB into the cell through the access transistors N3 and N4, and read mode, to read the data from the cell. For the writing and reading operations, the Word Line (WL) is made high so that N3 and N4 are connected to the memory cell. If WL is low, then the cell is under hold mode and has to retain its values at the output nodes Q and QB. However, at lower technology node processes, due to power leakage, the values at Q and QB may get disturbed. During hold mode, if Q=1 and QB=0, then, due to leakage current, the charged capacitor at node Q may get discharged through the N1 transistor. This makes the value at Q lower than Vdd and makes the pull-up transistor P2 switch ON, creating a wrong value at the QB node.

As TIGFET offers lower leakage power due to gate control, to overcome the read disturbance at lower channel lengths, the MOSFET is replaced with TIGFET [24] in the SRAM cell, as shown in Figure 6.

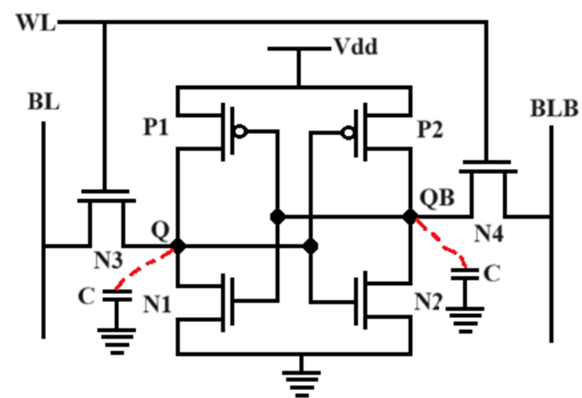

Fig. 5. 6T-SRAM using MOSFET.

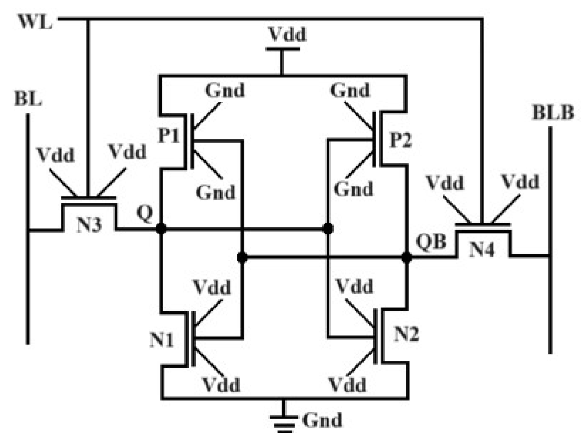

Fig. 6. 6T-SRAM using TIGFET.

Noise margin is a performance parameter that indicates how much noise or unwanted signal can be tolerated. Static Noise Margin (SNM), the measure of stability of SRAM, can be obtained as the side of a maximum square that can be fitted into the butterfly curves [25]. The stability analysis of SRAM is performed by measuring SNM at hold mode, read mode, and write mode. Figure 7 shows the experimental setup using TIGFET. Figure 7(1)(a, b) shows the hold mode for the top and bottom inverters. To operate under hold mode, WL is made low so that the access transistors are in the cut-off region. Figure 7(2)(a, b) represents the write 0 mode, and Figure 7(3)(a, b) shows the read mode for the two inverters.

IV. RESULTS AND DISCUSSION

The 6T SRAM using TIGFET was designed by applying proper biasing voltages and simulated at a Vdd of 1 V using the Synopsys HSPICE tool with TIGFET 10 nm, MOSFET 32 nm PDK models. The simulation results are shown in Table II. The drive current of TIGFET is more compared to MOSFET. The results show fewer write and read delays for the TIGFET-SRAM cell. The TIGFET is offering low OFF current and low leakage power compared to the MOSFET. The leakage power is reduced to 92.34% whereas the average power is reduced to 99.98% compared to MOSFET technology.

Transient analysis was performed for the SRAM using TIGFET for a period of 500 ns once it is stable. Figure 8 shows the transient response waveform. At 0 ns, WL=1, and a write operation is performed with Q=0 and QB=1. From 50 to 100 ns, a hold operation can be observed, in which Q and QB values remain unchanged. At 100 ns, a read operation is performed, where Q=0 and QB=1. Again at 200ns, WL is made high and a second write operation is performed with BL=1, so that Q=1 and QB=0 can be observed. The second read operation at 300 ns takes place by precharging BL and BLB to Vdd.

Read delay is the time taken by BL to discharge 50% of Vdd, and the discharging is taking place for the 0 read operation. For TIGFET-SRAM, read delay is 38.7ns, which is less compared to MOSFET technology.

The amount of time taken by the data at the internal node Q of SRAM to change according to the value at BL is known as the write delay. The write delay of TIGFET-SRAM is reduced to 33.44% compared to MOSFET, showing that the speed of operation is improved using TIGFET technology.

The stability analysis for the SRAM cell can be done in the hold, read, and write modes with the help of butterfly curves. SNM was measured from the butterfly curves, as shown in Figure 9. Table III shows a comparison of SNM values for MOSFET-based SRAM and TIGFET-based SRAM. The SNM values with TIGFET-SRAM are improved in all modes due to the lower leakage power offered by TIGFET. For the TIGFET-based SRAM, hold SNM has 16% improvement, read SNM is improved by 31.25%, whereas write SNM is improved by 68% compared to that of the MOSFET-based design.

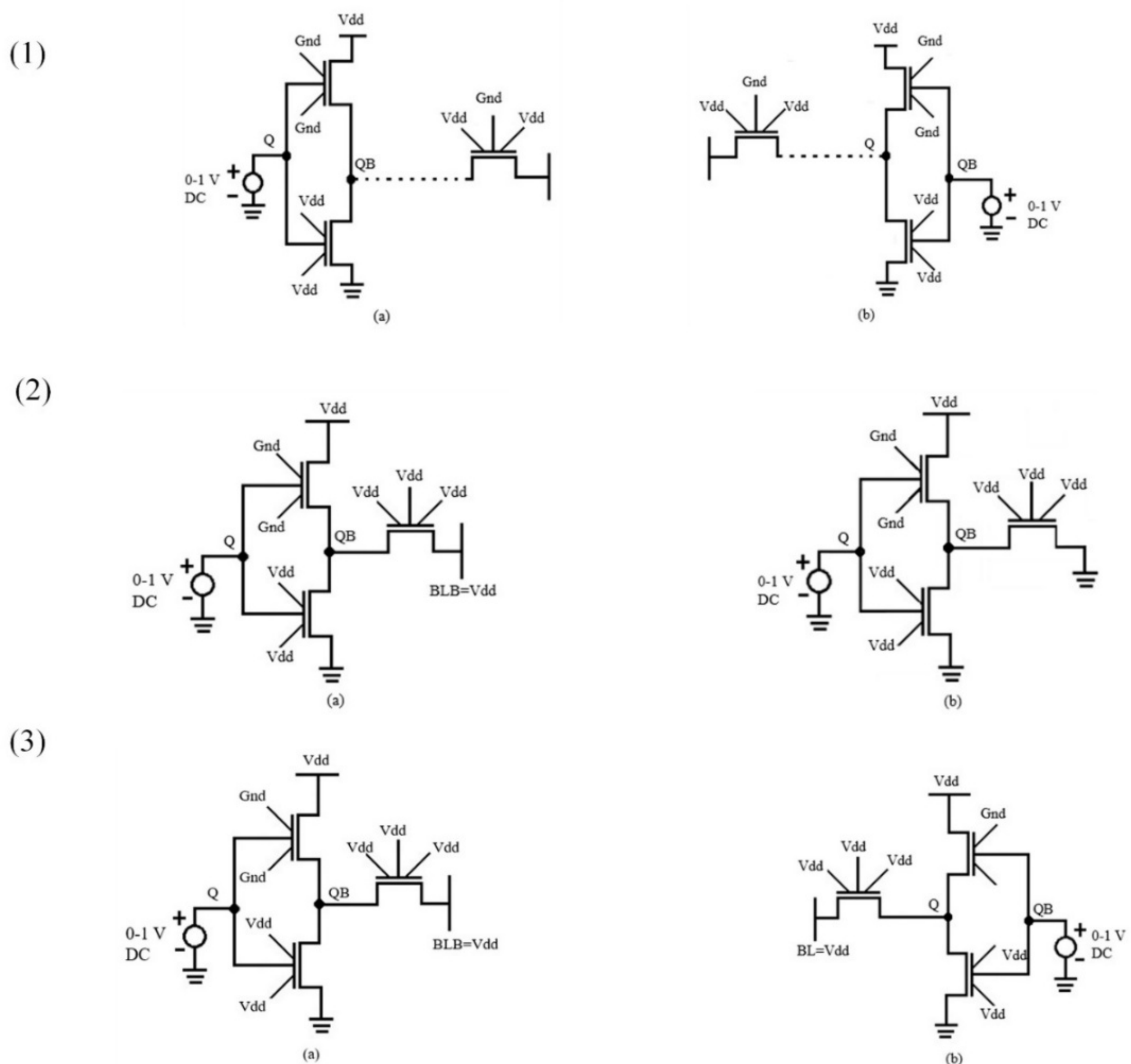

Fig. 7. Schematic of SNM measurement setup (1) Hold mode: (a) Top inverter (b) Bottom Inverter; (2) Write mode: (a) Top inverter (b) Bottom inverter; (3) Read mode: (a) Top inverter (b) Bottom inverter.

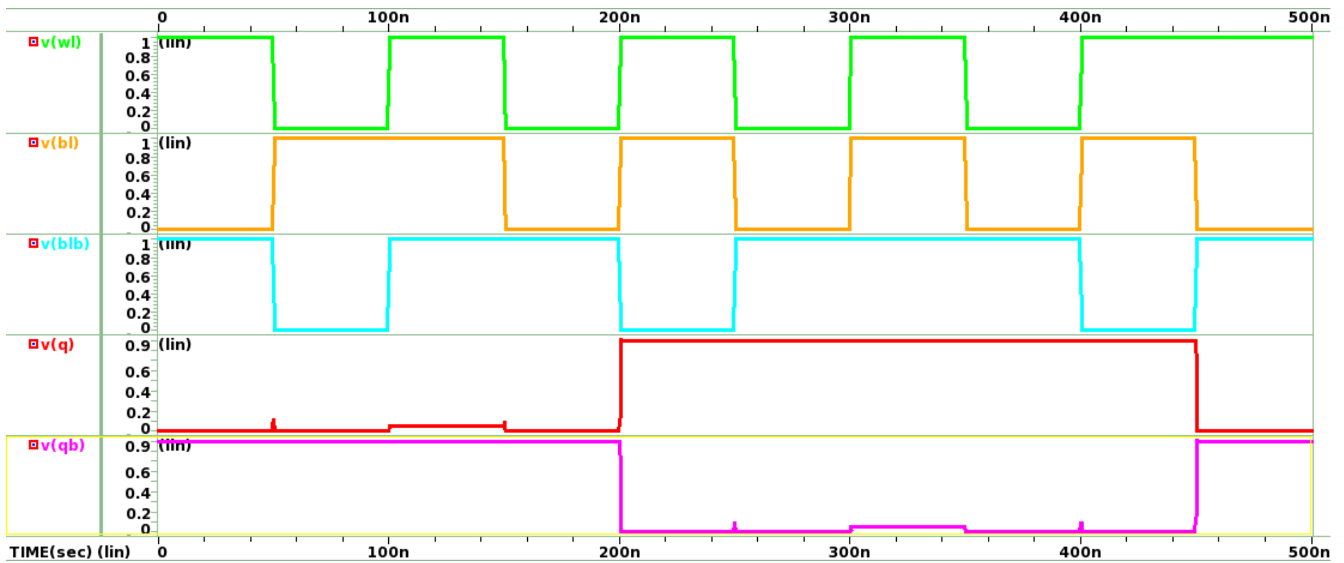

Fig. 8. Transient response of 6-T SRAM using TIGFET.

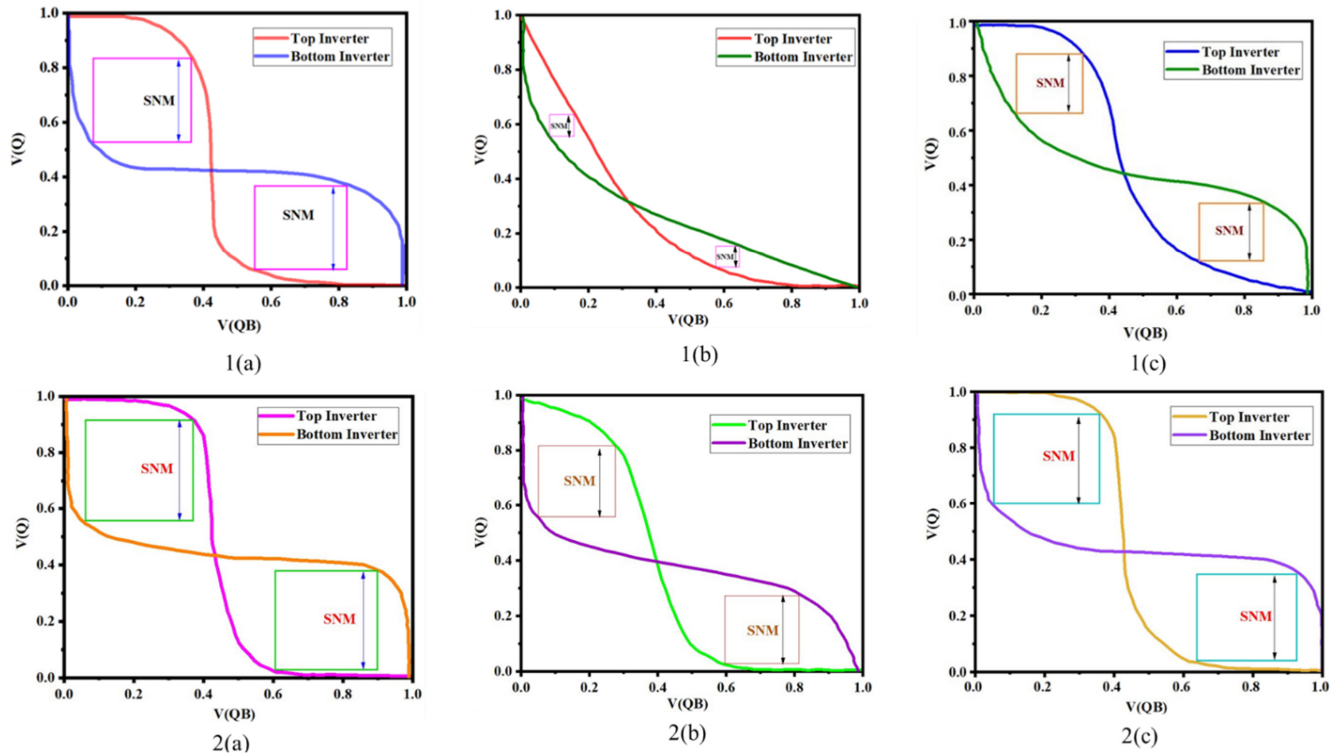

Fig. 9. SNM measurement of 6T-SRAM using Butterfly curves: 1 - MOSFET, (a) hold, (b) write, (c) read; 2- TIGFET: (a) hold, (b) write, (c) read.

TABLE II. COMPARISON OF CMOS-SRAM AND TIGFET-SRAM PARAMETERS

Type	Write-delay	Read-delay	Leakage power	Average power
TIGFET-SRAM-6T	40 ns	38.7 ns	12.37 pW	3.5626 nW
CMOS-SRAM-6T	60.1 ns	50.2 ns	161.60 pW	26.49 uW

TABLE III. COMPARISON OF SNM

Type	Hold SNM (V)	Read SNM (V)	Write SNM (V)
MOSFET 6-T SRAM	0.3	0.22	0.08
TIGFET 6-T SRAM	0.36	0.32	0.25

V. CONCLUSION

This paper presents the design and performance evaluation of an SRAM using TIGFET, including a detailed stability analysis. With stacked SiNWs as channel material and because of Schottky barriers near the source and drain terminals, TIGFET-SRAM shows better performance. TIGFET provides faster switching behavior with low carrier transit time, so that the speed of operation is faster. Quantitatively, the write and read delays of the proposed TIGFET-SRAM are reduced by 33.44% and 22.90%, respectively, compared to the MOSFET-SRAM. Furthermore, the stacked SiNW channel significantly minimizes leakage current, resulting in lower leakage and average power consumption. This improvement in power efficiency highlights the suitability of TIGFETs for low-power, high-speed memory applications.

In addition, the SNM analysis for hold, write, and read modes confirms that the TIGFET-SRAM provides improved stability and robustness under different operating conditions. Overall, the findings validate that TIGFET-based SRAM offers a compelling alternative to traditional MOSFET-based designs, combining enhanced speed, reduced power dissipation, and better noise immunity, making it a promising candidate for next-generation nanoscale memory systems.

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