A 4-4.8GHz Adaptive Bandwidth, Adaptive Jitter Phase Locked Loop

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***Abstract*—A low power, low phase noise adaptive bandwidth phase locked loop is presented in this paper. The proposed structure benefits from a novel lock status monitor unit (LSMU) that determines loop operation and loop bandwidth. The loop filter resistance and charge pump current are inversely proportional and bandwidth to reference frequency is maintained fixed. This structure is simulated in 0.18 µm CMOS technology and simulation results are presented.**

Keywords-low power; fast lock; adaptive bandwidth frequency synthesizer

I. INTRODUCTION

The increasing demand for high speed, low power, small size and portable electronic and communication devices is growing more and more. This mounting exigency has forced many electronics engineers to confront with several challenging problems. One of the most important building blocks in many high-speed, high-performance systems is phase locked loop (PLL). The basic duty of a PLL is to eliminate the phase difference between input and output waveforms and produce a pure output waveform with desired frequency. However, in many applications, the resulted waveform is not ideal. The digression of produced output and the ideal form is expressed in terms of phase noise and jitter.

There are several sources of noise in a PLL system such as input reference noise, phase and frequency detector (PFD) noise, charge pump (CP) noise, divider noise and especially voltage controlled oscillator (VCO) noise. In other words, each building block in a PLL produces a signal which is not ideal. So the overall system will suffer from different sources of noise. Mainly, these several sources are divided into two main categories: in-band and out-of-band phase noise [1]. In fact, it is shown in [1] that there are two different noise transfer functions for a PLL, one for the noise due to VCO (which is referred to output and has a high pass nature) and one for all other sources of noise (which is referred to input and has a lowpass nature). This means that for the frequencies inside the loop bandwidth, the loop will track the input referred noise and the VCO noise will be suppressed. On the other side, for the frequencies outside the bandwidth, the PLL noise approaches the VCO noise and the other sources of noise will not have an important role in output noise [1]. Thus, bandwidth choice will have an important role in determining the output noise of a PLL. On the other hand, several PLL characteristics such as settling behavior, stability and lock time are affected by PLL bandwidth.

The choice of PLL bandwidth will appear more and more confusing when we look into the PLL structure. A PLL has a discrete-time nature and in order to be able to approximate it with a continues time system, the bandwidth to the reference frequency ratio should be sufficiently small. In other words, if the bandwidth of the PLL is a significant fraction of the input frequency, continues time approximation will not be accurate [2]. So the first challenging step in the design procedure of a PLL is bandwidth choice. However, it is possible to select an optimum PLL bandwidth which satisfies all requirements. Unfortunately, the loop bandwidth of a PLL is a function of PVT variations and different loop parameters such as charge pump current, loop filter elements, VCO oscillation frequency, and dividing ratio. This means that any change in one of these parameters will result in bandwidth change and the optimum designed operation will be lost. In order to maintain the optimum performance, adaptive bandwidth PLL is a solution. The main idea in adaptive bandwidth PLL is to reform the PLL structure in such a way that the bandwidth to reference frequency ratio is kept fixed [2, 4]. This aim is usually reached using loop parameter variation according to loop conditions and dynamics. Several architectures have been proposed to achieve bandwidth adaptivity. In this work a new architecture is proposed which achieves adaptivity using a lock status monitor unit.

II. A REVIEW ON CHARGE PUMP PLL

Basically, a PLL is a feedback system in which the phase difference between input and output signals is eliminated and thus, the output and input frequencies will be equal (in absence of a divider in feedback path) [3]. However, in many applications, it is not possible to remove phase difference completely but the constant phase difference will also result in frequency equality.

$$\varphi_{out} - \varphi_{in} = Cons. \Rightarrow \frac{d\varphi_{out}}{dt} = \frac{d\varphi_{in}}{dt} \Rightarrow \omega_{out} = \omega_{in} \qquad (1)$$

Figure 1 depicts the basic structure of a charge pump PLL. The PFD compares the frequency and phase of its two inputs and produces an "up" or "down" signal at its output. In fact, if

the reference frequency is greater than the divided frequency, the output frequency of the VCO should increase and an "up" signal is generated. On the other hand, if the divided frequency is more than the reference frequency, the output frequency of VCO should decrease and a "down" signal is generated. According to the PFD output, the charge pump which basically consists of two totally matched current sources, will inject or draw current from the loop filter. The low pass filter (LPF) output, according to the sourced or sunk current, will force voltage controlled oscillator to increase or decrease its oscillation frequency. The divider will divide output frequency and deliver the result to the PFD. Obtaining the transfer function of every building block in PLL structure, one can show that the bandwidth of the PLL is as shown in (2) where ω_n and ξ are defined as (3) and (4) respectively. Because of complexity in (2), the two approximations are presented in (5) and (6) [1] .In these equations, I, K_{vco}, C_1, N, and R are charge pump current, VCO sensitivity, loop filter capacitance, divider ratio and loop filter resistance respectively.

$$\omega_{3dB} = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{4\zeta^4 + 4\zeta^2 + 2}} \quad (2)$$

$$\omega_n = \sqrt{\frac{I.K_{vco}}{2\pi N C_1}} \quad (3)$$

$$\zeta = \frac{R}{2}\sqrt{\frac{I.K_{vco}.C_1}{2\pi N}} \quad (4)$$

$$\omega_{3dB} \approx 2\zeta\omega_n, (\, for \zeta > 1.5) \quad (5)$$

$$\omega_{3dB} \approx (1 + \sqrt{2}\zeta)\omega_n, (\, for \zeta > 1.5) \quad (6)$$

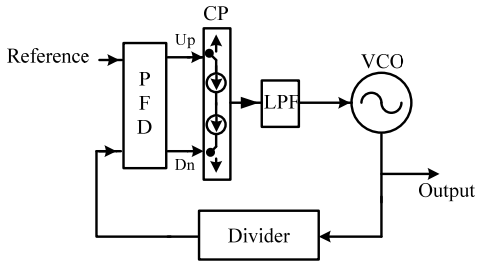

Fig. 1. Conventional PLL Structure

Several solutions have been proposed which have tried to achieve bandwidth to the reference frequency ratio. In [2], bandwidth adaptivity is obtained using two charge pumps and a ring oscillator. The key point in [2] is a symmetric load which is used in delay cells of the ring oscillator. The resistance of the symmetric load is changed using a control voltage that is generated using a bias generator. The proposed architecture in [2] exhibits ξ and ω_n/ω_{ref} ratio that are determined using a ratio of capacitors and thus are fixed. In [4], using an averaging linear varactor, I_{cp} and ω_{osc}^2 are inversely proportional together and in addition to the wide tuning range of LC-VCO, bandwidth adaptivity is obtained. However, these are two of most important reports in the literature. In fact, these are two most important and reviewed works in the fields but, in spite of their nobel ideas, there seem to be more issues to be addressed. In [2], the solution presented is only applicable for ring VCO based PLLs. However, in many high-performance systems, LC-VCOs are prefered due to best jitter performance. On the other hand, the solution in [4] seems to be a complex way to achieve bandwidth adaptivity.

III. PROPOSED ADAPTIVE BANDWIDTH PLL

As mentioned previously, in order to achieve adaptive bandwidth PLL, the ratio of bandwidth to the reference frequency should be kept fixed as much as possible. For many applications, the PLL is employed in overdamped condition [4]. This means that bandwidth approximation in (5) will be appropriate. So

$$\omega_{3dB} \approx 2\zeta\omega_n = \frac{R.I.K_{vco}}{2\pi N} \quad (7)$$

$$\frac{\omega_{3dB}}{\omega_{ref}} = \frac{R.I.K_{vco}}{2\pi N \omega_{ref}} \quad (8)$$

To maintain the best jitter performance, it is necessary to have fixed value for (8). With fixed values for N, ω_{ref}, and K_{vco}, if loop filter resistance "R" and charge pump current "I" are changed inversely, the required ratio will be achieved. It is necessary to mention that fixed K_{vco} requires a special VCO design with linear varactor which is described in D. Main building blocks of proposed structure are described in next sub-sections.

A. Phase Frequency Detector

The main function of PFD is to compare the phase and frequency of the reference waveform and the divider output and generate a suitable signal for the charge pump. In this work, a modified tristate PFD which is shown in Figure 2 is used.

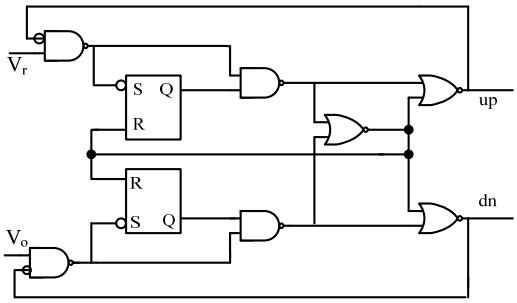

Fig. 2. Modified Tristate PFD

This circuit generates the reset signal (which is needed to prevent the unauthorized condition of "up=1 and down=1" in PFD) through a pass which does not include flip flops and so charge pump will not produce extra noise. One of the most important issues in PFD design is "dead zone". For small differences between PFD input signals, due to small differences

between rise time of latch outputs and reset path delay, PFD will not detect the phase difference and will not respond properly. In the designed PFD, the dead zone is tried to be minimized as much as possible [1]. Figure 3 depicts PFD characteristic. As it is obvious in Figure 3, the PFD exhibits a dead zone less than 0.36 degrees. It means that for phase differences between -0.18 and 0.18 degree this PFD will not respond accurately.

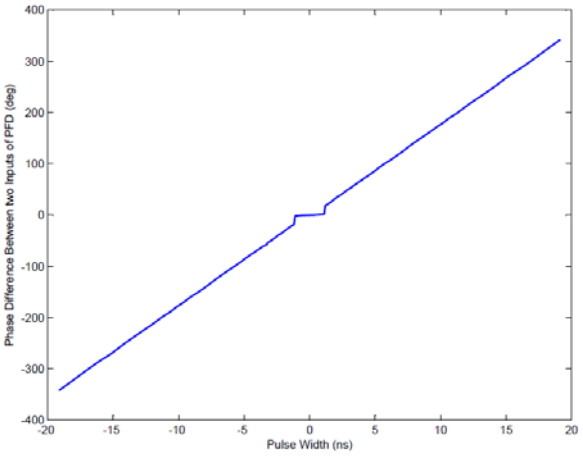

Fig. 3. PFD Characteristic

B. Charge Pump Circuit

In order to implement a charge pump with perfectly matched charge-discharge currents, a basic topology shown in Figure 4 was selected. This charge pump cell has two important advantages. First, in order to avoid channel length modulation effect and mismatch in output currents, an opamp is implemented in such a way that current mismatch issue is addressed. Second, the controlling switches are moved out of the signal path and comparing to conventional charge pump circuits, the required headroom of the circuit is decreased [1]. Actually, in order to have different charge pump current values, a charge pump with 5 cells similar to the circuit shown in Figure 4 were applied which were controlled using a controller. This controller will decide whether a charge pump cell is activated or not. Using this structure, an almost perfectly matched charge pump was obtained which plays an important role in adaptive bandwidth scheme and minimizing output jitter. Figure 5 depicts the final structure of the charge pump circuit. Note that all of the charge pump cells (CPCs) have the same structure but they do not produce the same current.

C. Loop Filter

In order to convert the charge pump current into VCO control voltage and eliminate its high-frequency components, a low pass filter is required. In proposed architecture, in order to achieve bandwidth adaptivity, loop filter resistance should change inversely with charge pump current. Figure 6 depicts proposed loop filter structure. Note that loop filter controlling signals are the same ones with charge pump topology. In this simple structure, as the charge pump current rises more resistances are paralleled with each other and hence, loop filter resistance is diminished. In addition, the C_2 capacitor is added in order to eliminate high-frequency ripple on the control line of VCO and its chosen one-tenth of the value of C_1 [1].

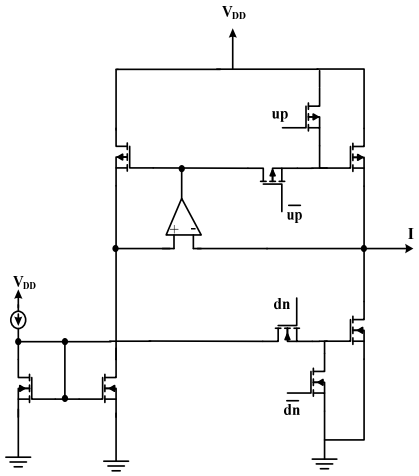

Fig. 4. Charge Pump Cell

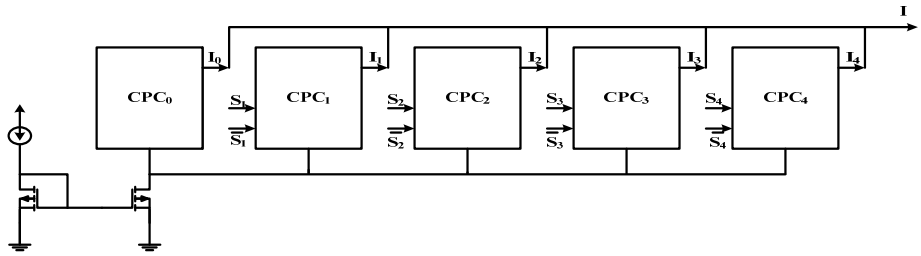

Fig. 5. Complete Charge Pump Structure

D. LC Voltage-Controlled Oscillator

A voltage controlled oscillator is a circuit that generates a periodic waveform that its frequency is determined by a control line. In PLL, the control line is LPF output. Basically, VCOs are divided into two main categories, ring VCO and LC VCO. In high-performance systems, because of superior noise operation, LC VCOs are preferred. The output frequency of a VCO is defined as (9) where K_{vco}, V_{ctrl}, ω_0, L, and C_v are VCO

sensitivity, control voltage, and free running frequency of VCO respectively.

$$\omega_{osc} = K_{vco}.V_{ctrl} + \omega_0 \quad (9)$$

As mentioned earlier, in order to achieve bandwidth adaptivity, a fixed K_{vco} oscillator is required. We applied an LC-VCO with linear MOSFET varactor. In fact, an averaging varactor which is implemented using MOSFETs that are biased in inversion region, similar to [4] is used to obtain a fixed K_{vco} architecture. Figure 7 demonstrates the averaging varactor structure. The DC voltages of the gates are chosen so that the nonlinearity of inversion region MOSFETs is averaged and the overall input capacitance of the varactor exhibits linear variations with respect to V_{ctrl}. Using this varactor in LC-VCO circuit shown in Figure 8, the resulted oscillator generates a sin waveform which its frequency varies from 4 to 4.8 GHz. Table I demonstrates the main performance parameters of LC-VCO.

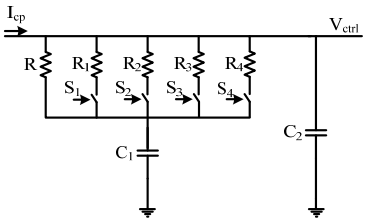

Fig. 6. Loop Filter.

E. Lock Status Monitor Unit

The lock status monitor circuit is the key controller unit of this structure. It is required to control the charge pump current and the loop filter resistance regarding the lock status of the loop. The LSMU circuit is shown in Figure 9. This circuit simply consists of four comparators. These comparators compare the control voltage of the LC-VCO with four reference voltages and produce four controlling signals. The comparison levels of comparators circuits are chosen according to simulation results. In fact, a conventional PLL with the same characteristics of our PLL was simulated first and critical levels of comparators circuits were obtained. The resulting control signals will control the loop filter resistance and the charge pump current of the PLL.

IV. SIMULATION RESULTS

Using all of the previously discussed building blocks, the final structure of adaptive bandwidth phase locked loop is shown in Figure 10. In order to examine the functionality of the proposed idea, a PLL with the same characteristics of proposed structure was simulated in Matlab Simulink and the idea was verified. Figure 11 shows the bandwidth to the reference ratio of this PLL for different values of the reference frequency. As its obvious from Figure 11, the bandwidth to the reference frequency ratio variations is decreased significantly in this PLL and consequently, the best jitter performance of the PLL will be preserved. Figure 12 depicts the RMS cycle-to-cycle jitter of this PLL. As it is shown, not only the RMS value of cycle-to-cycle jitter is reduced significantly, but also the jitter performance is maintained. This means that if the PLL is designed to have the minimum output jitter, its best performance will not be affected by any change in bandwidth. Figure 13 demonstrates the VCO control line of the proposed PLL when f_{ref}= 44MHz as an example. This PLL consumes less than 35mW power from 1.8 V supply voltage. Table II describes the most important characteristics fo this PLL.

TABLE I. LC-VCO CHARACTERISTICS

Technology	0.18µm
Supply Voltage (V)	1.8
Current Consumption (mA)	2.42
Tuning Range(GHz)	4 - 4.8
Free Running Frequency (GHz)	3.9
K_{VCO} (GHz/V)	1.05
Phase Noise @ 1MHz offset	-115 dBc/Hz

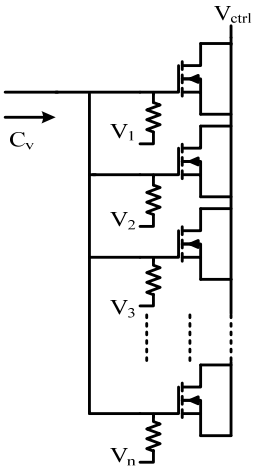

Fig. 7. Linear Varactor.

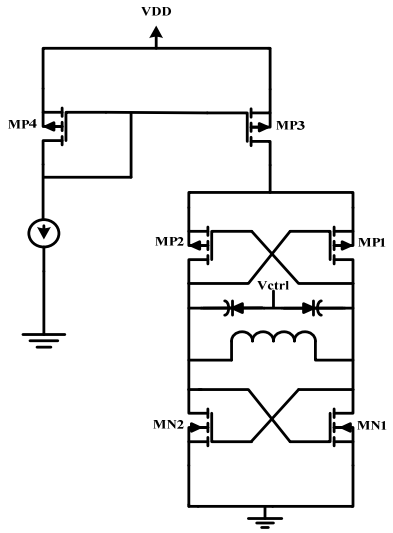

Fig. 8. LC VCO Structure.

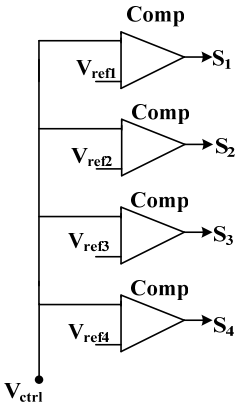

Fig. 9. Lock Status Monitor Unit (LSMU).

TABLE II. ADAPTIVE PLL CHARACTERISTICS.

Technology	0.18µm CMOS
Supply Voltage (V)	1.8
Power Consumption (mW)	47@ 4.8GHz
Cycle to Cycle jitter (ps)	0.45 @ 4.8GHz
Lock Time (µs)	Less than 10 (worst case)
Operating Frequency (GHz)	4-4.8

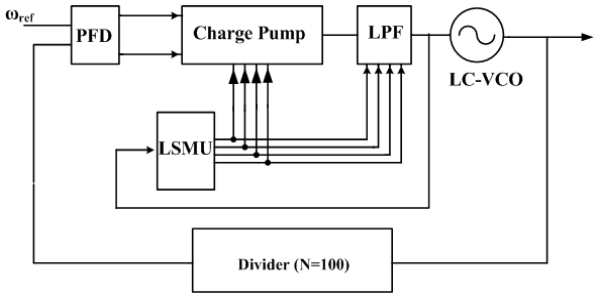

Fig. 10. Proposed Adaptive Bandwidth PLL Structure.

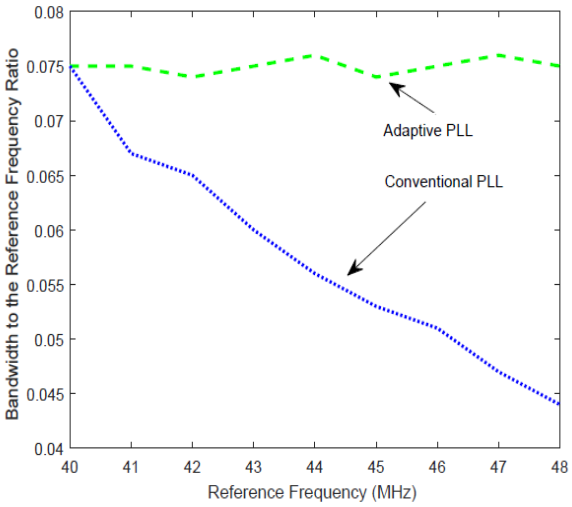

Fig. 11. Bandwidth to the Reference Frequency Ratio vs. Reference Frequency for Adaptive PLL (dashed line) and Conventional PLL (dotted line).

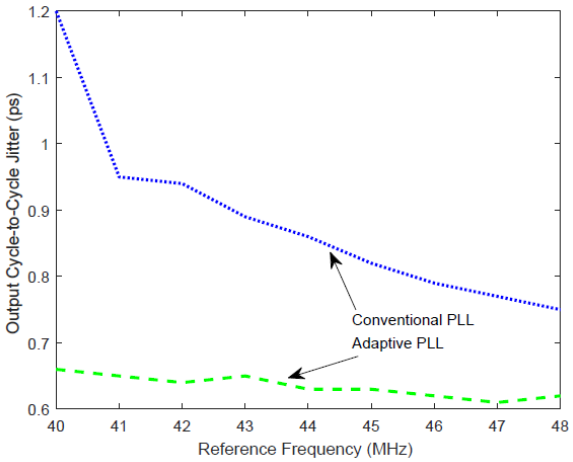

Fig. 12. Output Cycle-to-Cycle Jitter vs. Reference Frequency; Adaptive PLL (dashed line) and Conventional PLL, (dotted line)

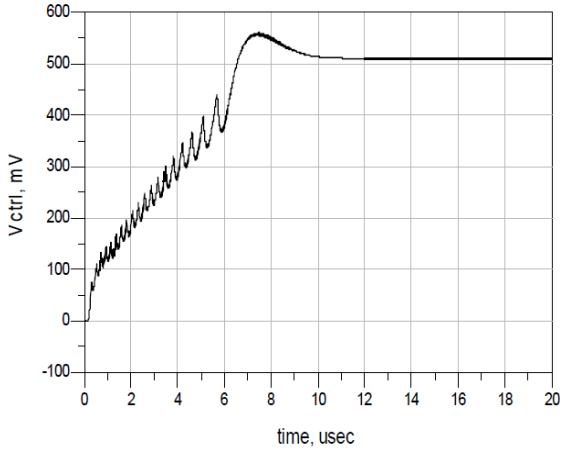

Fig. 13. VCO Control Voltage vs. time @ f_{ref}=44MHz

V. CONCLUSION

A 4-4.8 GHz adaptive bandwidth PLL is proposed and simulation results are presented. To achieve adaptivity, the charge pump current and the loop filter resistance are inversely proportional and therefore, the ratio of bandwidth to reference frequency variation is minimized. A lock status monitor unit determines the lock status of the PLL and decides about the amount of charge pump current and loop filter resistance. Based on the simple adaptive scheme presented in this brief, the best jitter performance and bandwidth to the reference frequency ratio is preserved.

REFERENCES

[1] J. Rogers, C. Plett, F. Dai, Integrated Circuit Design for High-Speed Frequency Synthesis, Artech House, 2006

[2] J. G. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, pp. 1723-1732, 1996

[3] B. Razavi, Design of Integrated Circuits for Optical Communications, Mc Graw Hill, 2003

[4] T. Wu, P. K. Hanumolu, K. Mayaram, U. Moon, "Method for a Constant Loop Bandwidth in LC-VCO PLL Frequency Synthesizers", IEEE Journal of Solid-State Circuits, Vol. 44, No. 2, pp. 427 – 435, 2009