Offline Analysis of a Modified dqPLL Architecture based on THD Compensation Blocks for Three-Phase Grid-Tied Inverters

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Received: 11 January 2025 | Revised: 10 February 2025 and 24 February 2025 | Accepted: 27 February 2025

 DOI: https://doi.org/10.48084/etasr.10206

ABSTRACT

The control of electrical energy in intelligent smart grids is an important task that takes place in the control and synchronization block of the connected inverters, even for three-phase smart grids, because the supplied three-phase voltage source is distorted and contains disturbing harmonics that need to be filtered. In general, Phase-Locked Loops (PLLs) are the most widely used circuits to address this problem due to their high-speed controllability of the grid voltage and their direct influence on the Grid-Side Converter (GSC). This paper presents a new PLL architecture, based on the classical synchronous reference frame PLL (dqPLL), and aimed at filtering harmonics from the input signal for a three-phase smart grid application, structure. Our proposed architecture for harmonic filtering demonstrates its efficiency compared to the classical dqPLL by inserting a real three-phase vector acquired from a real three-phase voltage source. A comparative study of the results obtained between the two PLL architectures is presented and shows the effectiveness of our proposed structure by providing full compensation of the Total Harmonic Distortion (THD) from 9.052% to 0.36%.

Keywords-smart grids; Phase-Locked Loop (PLL); grid side converter; inverters; synchronous reference frame Phase-Locked Loop (dqPLL)

I. INTRODUCTION

The use of smart grids has been gradually increasing over the past few years, and the demand for electricity is also increasing due to the improved controllability of distributed power within these grids. This is further amplified in multi-source smart grids, as users can utilize various renewable energy sources to consume otherwise wasted energy. However, excessive power consumption can disrupt the grid, particularly when non-linear loads are connected. This disruption is primarily caused by harmonics present in the source signal and variations in its frequency. In multi-source smart grids, the same disturbances can occur at the Point of Common Coupling (PCC) between the main grid and the renewable energy sources, potentially distorting the signal and even causing disconnections between the different energy sources. Therefore, filtering these harmonics is necessary to improve the power quality of the grid source [1, 2]. Several research projects have proposed solutions and techniques for filtering these distorting harmonics from the distributed grid signal. There are two main approaches to address this problem: frequency-domain methods and time-domain methods. Frequency-domain methods include filtering techniques such as the Fast Fourier Transform (FFT) [3] and the Discrete Fourier Transform (DFT) [4], which provide speed and

resilience against noise, harmonics, and frequency variations. The Kalman filter [5] also falls into this category, providing an optimal balance between transient response and noise rejection for synchronous signals. Time-domain methods are divided into two types: open-loop and closed-loop. Open-loop methods include arctangent filtering techniques [6] and Space Sector Filtering (SVF) [7].

In general, frequency-domain approaches are better suited for harmonic monitoring and measurement due to their settling time of at least one cycle but they require larger data storage and computational resources. Time-domain methods, such as Zero-Crossing Detection (ZCD) [8], Weighted Least Square Estimation (WLSE) [9], Adaptive Notch Filtering (ANF) [8], and Phase-Locked Loop (PLL) techniques [10], have proven to be well suited for real-time grid control. Closed-loop approaches can provide greater accuracy and controllability by incorporating one or more control loops. In particular, PLLs have a long history in signal detection due to their simple design and great flexibility for a variety of problems, and they have long been recognized for their utility in grid frequency and phase detection. The classic and well-known PLL for frequency and phase detection in three-phase grids is the Synchronous Reference Frame PLL (SRF PLL) [11-14], also known as the dqPLL. Although it is effective for normal symmetric grids, it exhibits noise when detecting the fundamental frequency of harmonically distorted three-phase voltage sources.

Harmonics are generated by non-linear loads connected to the grid [15, 16]. This work focuses on the compensation of odd-order harmonics (5th, 7th, 11th, and 13th), as these are the most significant due to their higher amplitudes in the distributed signal, causing disturbances. It is therefore necessary to filter out these harmonics in order to reduce the Total Harmonic Distortion (THD) value. The THD at the rated output of the inverter should not exceed 5% [17], as specified in the EN50160 standard. Several research projects have focused on modifying the classical dqPLL architecture to mitigate the effects of harmonic noise and to accurately detect the fundamental grid frequency and phase. One example is the Double Second Order Generalized Integrator PLL (DSOGI PLL) [18], which, however, exhibits oscillations due to harmonics and DC offset, as well as overshoots in phase estimation and a delayed settling time. As an improvement to the DSOGI PLL, the Multiple Second-Order Generalized Integrators PLL (MSOGI PLL) [19] uses multiple parallel SOGI subsystems to extract individual harmonics and requires the number of SOGI subsystems to match the number of significant harmonics. While this technique can provide good results for harmonic filtering, it is susceptible to frequency variations. Another technique, the Harmonic Interharmonic and DC Offset PLL (HIHDO PLL) [20], provides instantaneous and accurate calculation of the required grid components, but exhibits a low overshoot in the dynamic response for magnitude and frequency. Finally, the Multi-Sequence Harmonic Decoupling Cell PLL (MSHDC PLL) [21, 22] enables fast identification and estimation of magnitude, phase, and frequency under harmonically distorted grid conditions, but its numerous Park transformation blocks increase processing time.

Previous PLL architectures have focused on filtering harmonics from the distorted voltage signal. The main challenge is to reduce the THD to a level that allows for accurate detection of the grid components. In this paper, we present a novel, improved, and modified architecture based on the classic dqPLL, which is capable of detecting the fundamental grid frequency and filtering the most significant successive-order harmonics (5th, 7th, 11th, and 13th). Due to its limited number of Park transformation blocks, our proposed architecture offers a reduced computational burden compared to the MSHDC PLL. As a selective harmonic detector and compensator, it employs multiplier blocks that operate on the phase angle of the dqPLL, with each block dedicated to a specific harmonic and independent of the others, unlike the MSHDC PLL where each harmonic is dependent on the others. We demonstrate the effectiveness of this modified dqPLL architecture, compared to the classical dqPLL, in terms of harmonic filtering and THD reduction. This comparison is performed first on a three-phase distorted signal generated in MATLAB, and then on a real three-phase voltage vector acquired from a real three-phase voltage source. Real-time data acquisition is performed using an NI ELVIS II device as the hardware interface and LabVIEW for the software programming.

II. CLASSIC DQPLL STRUCTURE

The classic dqPLL architecture, also known as the SRF PLL, is widely used for frequency and phase detection in three-phase grids due to its simple design [11-14]. This architecture employs Clarke and Park transformations to convert the three-phase abc reference frame to a dq synchronous reference frame, thus simplifying the calculations. One of the resulting vectors, the *Vd* signal, is used to determine the input signal amplitude, whereas the other vector, the *Vq* signal, is driven to zero by a PI regulator. This *Vq* signal is then used to extract the frequency and subsequently the phase angle when the loop is closed. The PI regulator acts as a filter, and its output controls the oscillator providing the estimated phase angle. The phase error between this estimated phase angle and the initial grid phase angle then controls the dqPLL loop. The general structure of the classical dqPLL is shown in Figure 1 [12]. The equation for the transformation from the abc frame to the dq frame is shown in (1), and the equations for the *Vd* and *Vq* signals are shown in (2) and (3).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos(\theta_{PLL}) & cos\left(\theta_{PLL}-\frac{2\pi}{3}\right) & cos\left(\theta_{PLL}-\frac{4\pi}{3}\right) \\ -sin(\theta_{PLL}) & -sin\left(\theta_{PLL}-\frac{2\pi}{3}\right) & sin\left(\theta_{PLL}-\frac{4\pi}{3}\right) \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (1)$$

$$V_d = V_m \cos(\theta_{grid} - \theta_{PLL}) \quad (2)$$

$$V_q = V_m sin(\theta_{grid} - \theta_{PLL}) \quad (3)$$

where θ_{grid} is the initial phase angle of the grid voltage source, θ_{PLL} is the estimated grid phase angle at the output of the dqPLL, and V_m is the maximum amplitude of the grid voltage source. When the dqPLL loop is closed, θ_{grid} is approximately equal to θ_{PLL}.

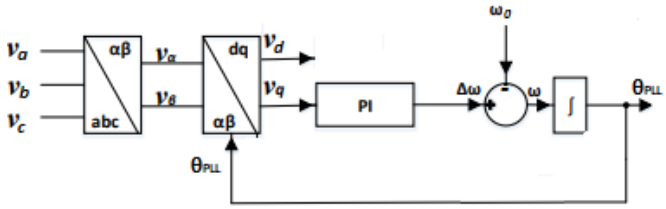

Fig. 1. Classic dqPLL structure.

III. MODIFIED DQPLL STRUCTURE

We have modified the classic dqPLL structure to accommodate the harmonic distortions present in the power source and to accurately detect the fundamental frequency under these conditions. Our goal is to reduce the THD to an acceptable level of less than 5%. To achieve this, we have added a harmonic compensator block that contains several sub-blocks, each dedicated to extracting and filtering a specific harmonic order. We focused on filtering the most significant successive-order harmonics (5th, 7th, 11th, and 13th), although the structure can accommodate additional sub-blocks for other harmonics. The general structure of the modified dqPLL is shown in Figure 2, where the modified dqPLL structure filters harmonics from the input signals *Vα* and *Vβ*, *Vα** and *Vβ**, represent the filtered output signals.

The compensator block consists of four sub-blocks, each dedicated to extracting and filtering one of the four significant harmonics. Each sub-block contains a multiplier gain that multiplies the phase angle at the dqPLL output to match the rotation speed of the target harmonic's phase angle. This modified phase angle adjusts the rotation speed of the *N*th-order harmonic's synchronous reference frame in the $(\alpha\beta/dq)_N$ transformer, which follows the multiplier gain in the compensator sub-block, as shown in Figure 3. When the $(\alpha\beta/dq)_N$ transformer's synchronous reference frame rotates at the target harmonic's frequency, the corresponding harmonic's alternating signal becomes a DC signal. Consequently, the $(\alpha\beta/dq)_N$ transformer's output signals contain primarily the fundamental component and the remaining harmonics, which are then filtered by the sub-block's low-pass filter. Finally, the inverse transformation $(dq/\alpha\beta)_N$ reproduces the *N*th-order harmonic, which is subtracted from the original $(\alpha\beta)$ input signals.

The outputs of the four sub-blocks, representing the filtered harmonics, are summed. This sum is then subtracted from the original *Vαβ* signals in the main dqPLL loop. The resulting *V'alphabeta* signals represent the signals after the filtering and summation process. These are then subtracted from the original *Valphabeta* signals in the dqPLL loop to produce the final filtered outputs, *Vα** and *Vβ**, as shown in Figure 2. When the V_q signal of the classical dqPLL is forced to zero, the V_d signal will be equal to the V_m signal in (2) and (3), and the phase error will be zero under ideal grid voltage conditions. However, with harmonic distortion, the phase error will be non-zero due to the presence of harmonic frequency components that must be filtered. To perform this filtering, we use the following (4) and (5) to calculate the filtered *Vαβ** signals:

$$V_{\alpha\beta(filtered)} = V_{\alpha\beta} - (V_{\alpha\beta5} + V_{\alpha\beta7} + V_{\alpha\beta11} + V_{\alpha\beta13}) \quad (4)$$

$$V_{\alpha\beta i} = \left[T_{dq}(\mathrm{i})\right][f(s)]\left[T_{dq}(\mathrm{i})\right]^{-1} \quad (5)$$

where $V_{\alpha\beta i}$ represents the filtered output signals for each *i*th harmonic. In this study, we have selected i = (5, 7, 11, 13) as the desired harmonics to filter. $\left[T_{dq}(\mathrm{i})\right]$ represents the *dq* transformation of the *Vαβ* signals for each *i*th harmonic, and $[f(s)]$ is the transfer function of the low-pass filter.

IV. HARDWARE ACQUISITION METHOD

In this section we describe the hardware and software used to acquire the real three-phase grid voltage vector.

A. Acquisition Board

To acquire a real three-phase voltage vector from a real grid voltage source, we used the NI ELVIS II device [23]. This electronic board offers good performance and includes 16 analog inputs with 16-bit resolution and a sampling rate of 1.25 mega-samples per second.

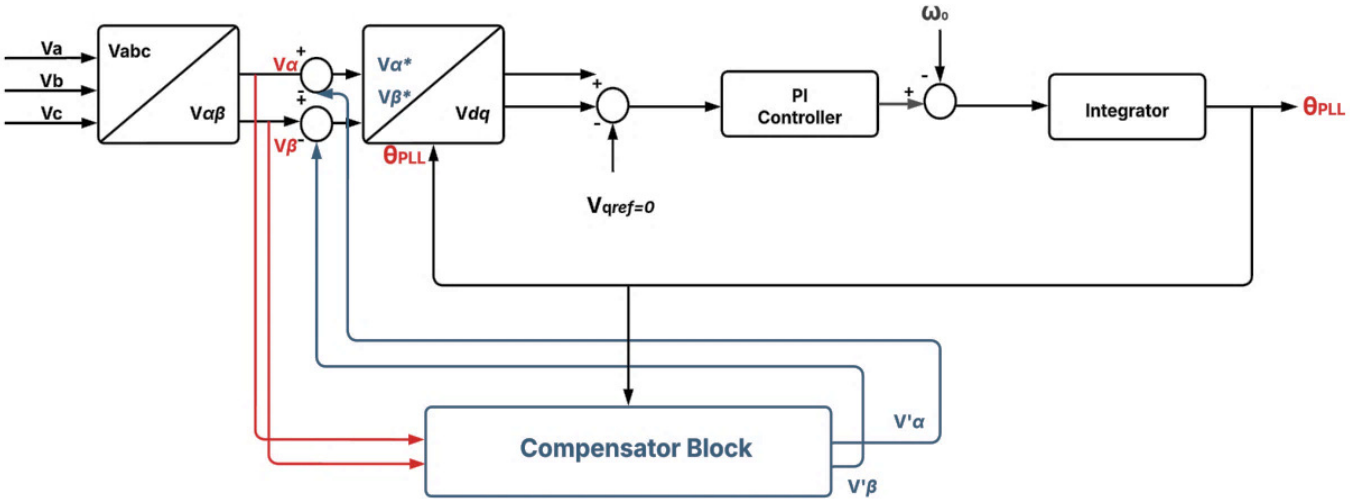

Fig. 2. Modified dqPLL structure.

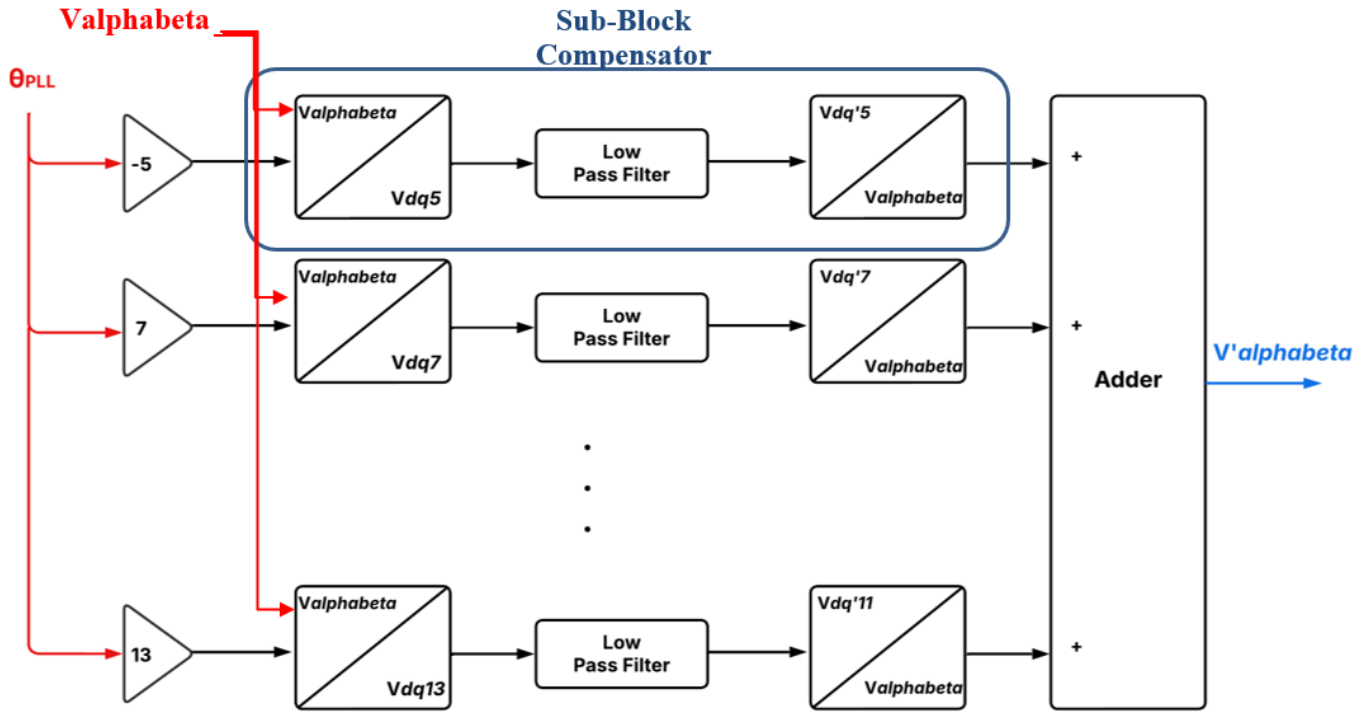

Fig. 3. Compensator block structure.

B. Power Adaptation Circuit

For the practical implementation, we connected the NI ELVIS II board to a power adaptation circuit. This circuit, consisting of three transformers and voltage dividers, reduces the main power source voltage from 220V to 12V, the required supply voltage for the NI ELVIS II device. The power adaptation circuit connected to the NI ELVIS II unit is shown in Figure 4 [24, 25], and a photograph of the actual setup is shown in Figure 5, illustrating the connection between the power source, the PC, the NI ELVIS II device, and the power adaptation circuit. The acquired three-phase voltage vector, shown in Figure 6, oscillates between 324 V and -324 V and exhibits deformation due to the presence of harmonics. Figure 7 shows a spectral analysis of the harmonic content of the acquired real signal vector, performed using MATLAB Simulink. The spectrum in Figure 7 clearly shows the presence of significant harmonics, specifically the 5th, 7th, 11th, and 13th order harmonics with amplitudes of 48 dBm, 35 dBm, 14 dBm, and 24 dBm, respectively.

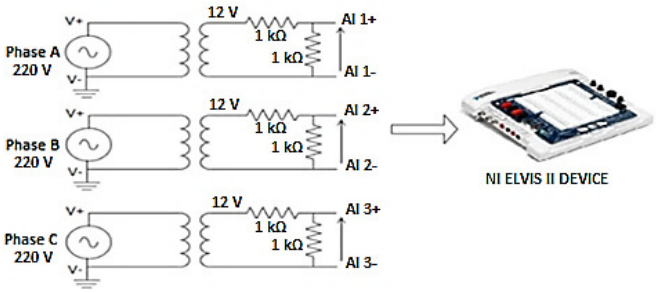

Fig. 4. Electrical acquisition circuit and NI ELVIS II device.

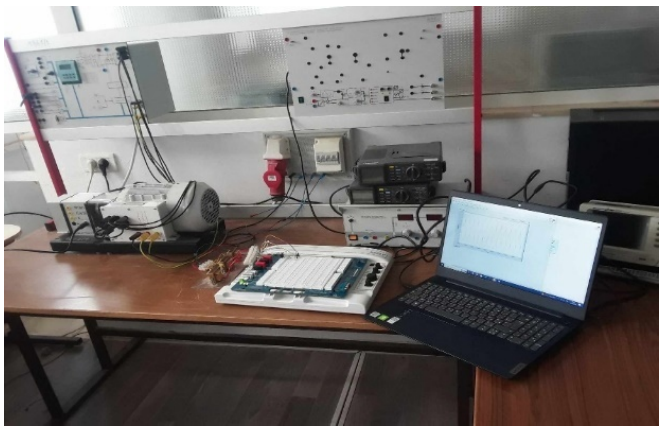

Fig. 5. Practical experiment of the vector acquisition process.

C. LabVIEW Programming Code

For the signal vector acquisition program, we used LabVIEW to develop a graphical interface. The NI ELVIS II device served as the data acquisition board, utilizing analog inputs AI0, AI1, and AI2 to acquire the three-phase voltage signal, *Vabc*. Within LabVIEW, using the DAQmx toolkit, we cascaded three "Create Channel" functions to open these analog inputs. The "DAQmx Timing" function was configured to acquire 10,000 samples per second. The "DAQmx Read" function then read 10,000 samples from the three channels. The resulting graphical interface is shown in Figure 8.

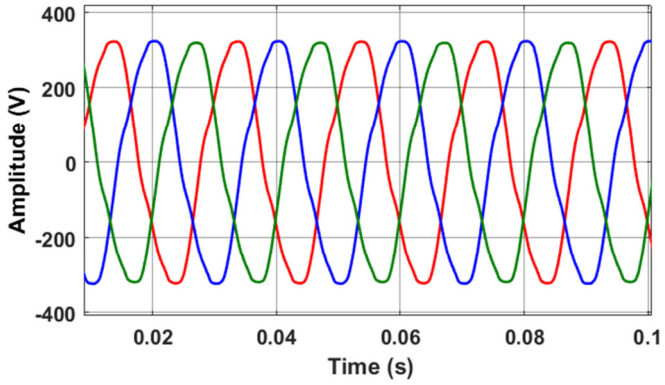

Fig. 6. Acquired real three-phase signal vector.

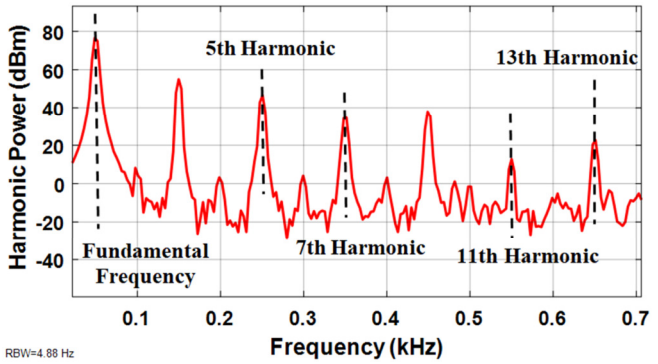

Fig. 7. Harmonic power spectrum of the acquired real three-phase signal vector.

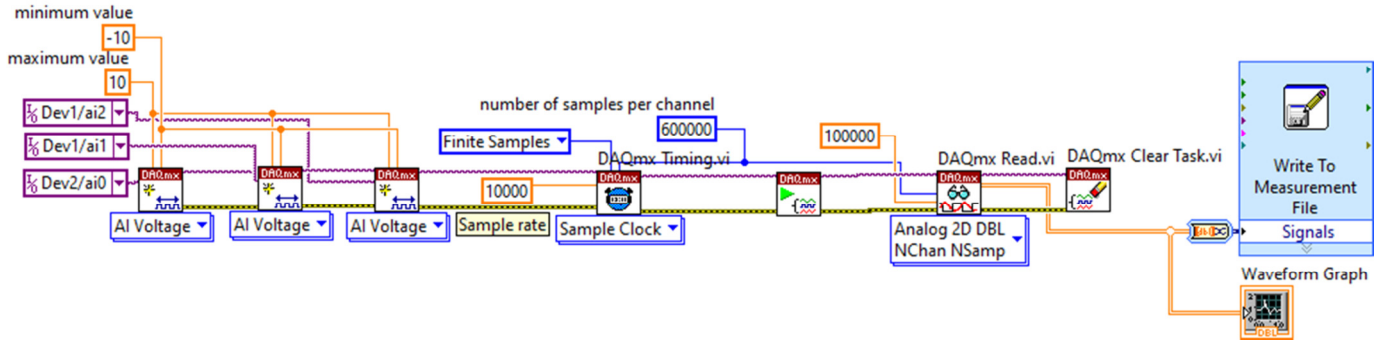

Fig. 8. LabVIEW code used for the signal vector acquisition.

V. OFFLINE ANALYSIS AND SIMULATION RESULTS

In this section, we present a comparative analysis of the modified dqPLL structure and the classical dqPLL, based on MATLAB simulation results obtained after their respective designs. The simulation results are divided into two parts, corresponding to the two experiments conducted: first, using a distorted three-phase signal generated by MATLAB as input to each dqPLL type, and second, using a three-phase voltage vector acquired from a real three-phase grid. For the MATLAB-generated signal, we used an ideal three-phase generator and introduced harmonics by adjusting the generator block's parameters. The harmonics considered were the 5th, 7th, 11th, and 13th orders, each with a magnitude equal to 10% of the maximum input voltage amplitude. For both dqPLL architectures and both experiments, the PI regulators used the same parameter values, specifically kp=1.357 and ki=304.61, which were chosen for optimal performance.

A. Simulation Results using MATLAB Generated Signal

After generating the distorted three-phase signal, we applied it to the input of each dqPLL architecture and initiated the simulations. First, we examined the performance and frequency response of the classical dqPLL under these harmonic distortion conditions. The frequency response of this classical dqPLL architecture is shown in Figure 9. As can be seen in the figure, the classical dqPLL fails to accurately detect the fundamental frequency of the 50 Hz input voltage source, oscillating significantly around this value. This necessitates a modification to the architecture in order to improve performance. The frequency responses of both the classical and modified dqPLL architectures under the same harmonic distortion conditions are shown in Figure 10, and Figure 11 provides a zoomed-in view of the last 100 ms of the simulation results shown in Figure 10. As illustrated in Figure 11, the modified architecture (blue curve) significantly improves the response compared to the classical dqPLL (red curve), reducing the oscillations around 50 Hz and achieving a settling time of 0.09 s (Figure 10).

The classical dqPLL's frequency response exhibits settling instability due to the harmonic distortion in the input signal, oscillating around 50 Hz with a deviation of ±24.5 Hz (±49% relative to the center frequency) in the steady state. Conversely, our modified dqPLL architecture provides a much more stable settling frequency, oscillating by only ±0.04 Hz (0.08% relative to the center frequency) under the same harmonic distortion.

In conclusion, the modified dqPLL architecture improves frequency stability, providing better immunity to harmonic distortions. We then analyzed the harmonic power spectrum at the outputs of both the classical and modified dqPLL architectures. The harmonic power spectrum of the output signals is shown in Figure 12. As can be seen in the figure, the modified dqPLL architecture (blue curve) significantly attenuates the harmonic power compared to the classical dqPLL architecture (red curve) while preserving the fundamental frequency. Specifically, the 5th harmonic power is attenuated by 57 dBm, the 7th by 60.5 dBm, the 11th by 52.5 dBm, and the 13th by 50.15 dBm.

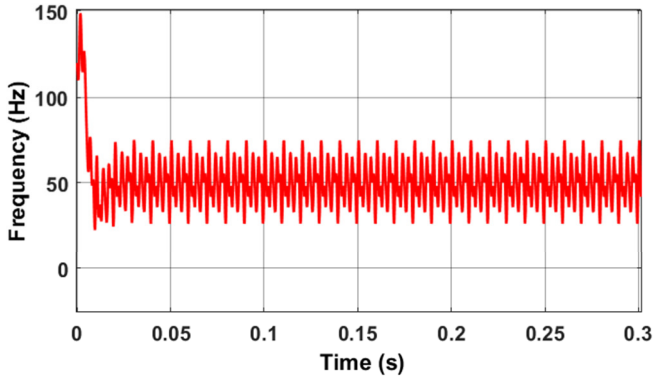

Fig. 9. Frequency response of the classic dqPLL.

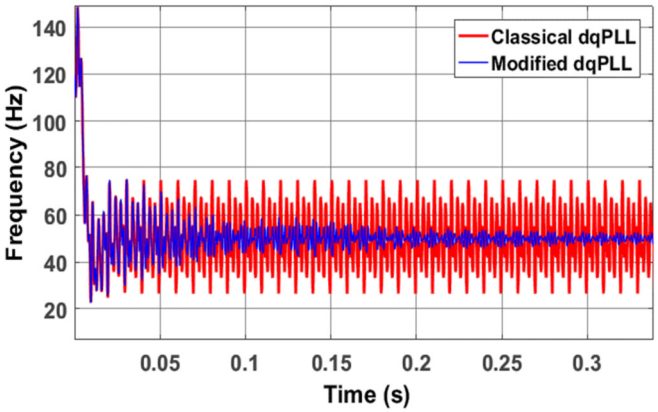

Fig. 10. Frequency responses of the two dqPLL architectures.

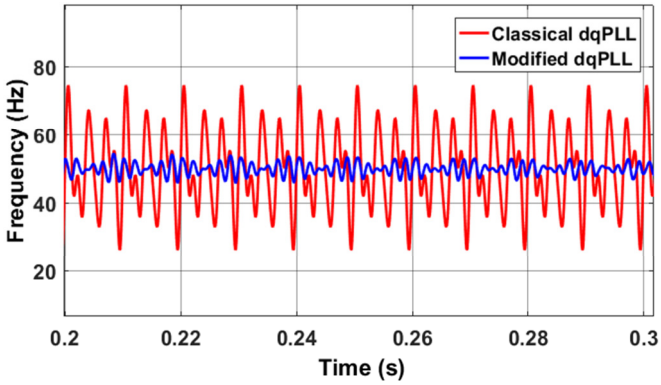

Fig. 11. Zoom on the last 100 ms of the frequency responses of the two dqPLL architectures.

Table I presents a comparative analysis of the output harmonic power for both the modified and classical dqPLL architectures under the same input voltage conditions. Table I clearly demonstrates the efficiency of the modified dqPLL architecture in reducing harmonics compared to the classical architecture, reducing the THD value from 14.36% to 0.039%. This THD value is significantly lower than that achieved by the classical dqPLL structure.

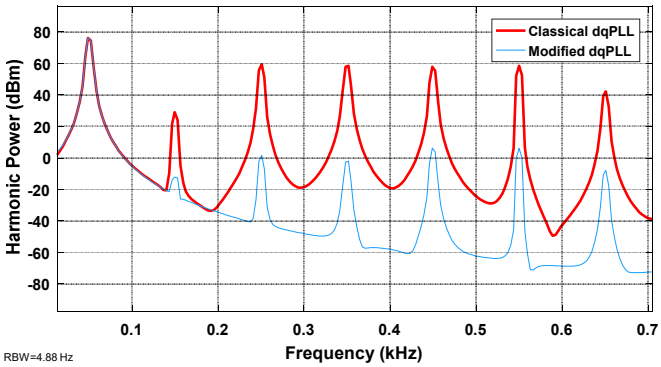

Fig. 12. Harmonic power spectrum.

TABLE I. COMPARATIVE ANALYSIS OF OUTPUT HARMONIC POWER FOR CLASSICAL AND MODIFIED dqPLL ARCHITECTURES

Harmonic	Input phase voltage source power (dBc)	Output power (dBc)	
		Classical dqPLL structure	Modified dqPLL structure
1	76.10 (dBm)	76.08 (dBm)	76.10 (dBm)
2	-Inf	-Inf	-Inf
3	-Inf	-47.14	-88.33
4	-102.06	-105.33	-Inf
5	-19.42	-16.60	-74.59
6	-97.66	-93.96	-Inf
7	-20.37	-17.51	-78.14
THD (dBc)	-16.86 (14.36%)	-12.63 (23.35%)	-68.04 (0.039%)

B. Simulation Results using a Real Three-Phase Signal Vector

After acquiring the voltage vector using LabVIEW, we processed it in MATLAB. To introduce the acquired real signal vector into MATLAB, we used a signal builder block to convert the data from abc values (imported from an Excel sheet via LabVIEW) into signals. Since the voltage amplitude of the obtained signals was between -10 V and 10 V, we added a multiplier gain to scale the amplitude between -324 V and 324 V. The output of the signal builder block was then connected to the input of each dqPLL structure designed in MATLAB. The simulation time step was set to 0.0001 s for higher resolution.

Both PLL types were implemented in MATLAB using identical simulation parameters and PI controller settings for their respective main loops. After processing the acquired three-phase voltage vector, we confirmed that the signal was distorted by harmonics and had a fundamental frequency of 50 Hz. The improvement achieved by each dqPLL type can be seen in the output frequency and frequency spectrum by comparing one phase of the acquired vector with the corresponding output signals.

We first connected each dqPLL structure to the acquired signal vector, and the resulting output frequency responses of the two dqPLL structures are shown in Figure 13. The red curve represents the frequency response of the classical dqPLL and the blue curve represents the frequency response of the modified dqPLL, indicating a reduction in noise compared to

the classical dqPLL with a settling time of approximately 0.8 s. Figure 14 shows a zoomed-in view of the last 100 ms of the simulation results in Figure 13. As can be seen in Figure 14, the classical dqPLL structure exhibits a frequency error ($\Delta\varepsilon$) of ±3 Hz around the fundamental frequency. In contrast, the modified structure reduces this error to ±0.4 Hz, clearly demonstrating its effectiveness in mitigating unwanted oscillations and noise.

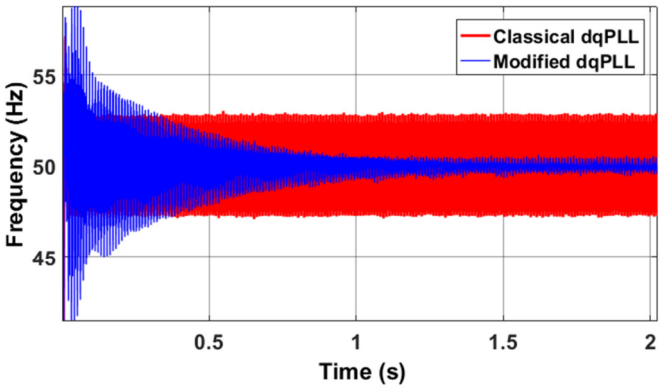

Fig. 13. Frequency responses of the two dqPLL architectures.

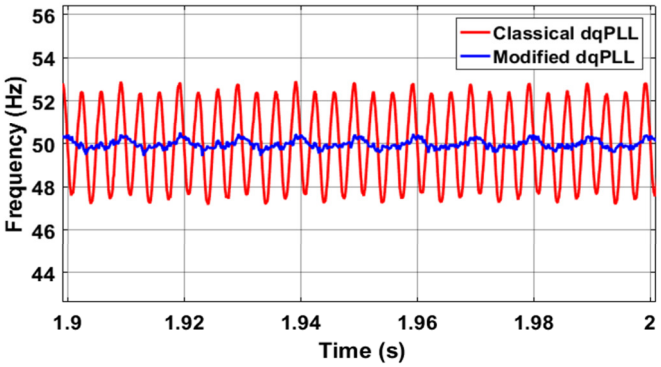

Fig. 14. Zoom on the last 100 ms of the frequency responses of the two dqPLL architectures.

We then analyzed the frequency spectrum of one phase of the input voltage vector and the outputs of both the classical and modified dqPLL structures to compare the harmonic power levels, as shown in Figure 15. This figure shows the power (dBm) of each harmonic as a function of frequency (kHz) for one phase of the input voltage vector (gray curve), the output of the classical dqPLL (red curve), and the output of the modified dqPLL (blue curve). Comparing the input and output of the modified dqPLL, we observe that the fundamental frequency is preserved, whereas the 5th harmonic is reduced by 25.6 dBm, the 7th by 24.4 dBm, the 11th by 3.2 dBm, and the 13th by 8.8 dBm. This clearly demonstrates the effectiveness of the modified structure in reducing the power of each significant harmonic.

Table II shows a comparative analysis of the harmonic power for one phase of the input voltage source vector and for the outputs of the classical and modified dqPLL structures together. It can be observed that using the same input voltage source (with a THD of 9.052% for one analyzed phase) for both dqPLL structures, the modified dqPLL reduces the power of each significant harmonic, thus reducing the total THD from 9.052% to 0.36%. This THD value is significantly lower than that achieved by the classical dqPLL structure.

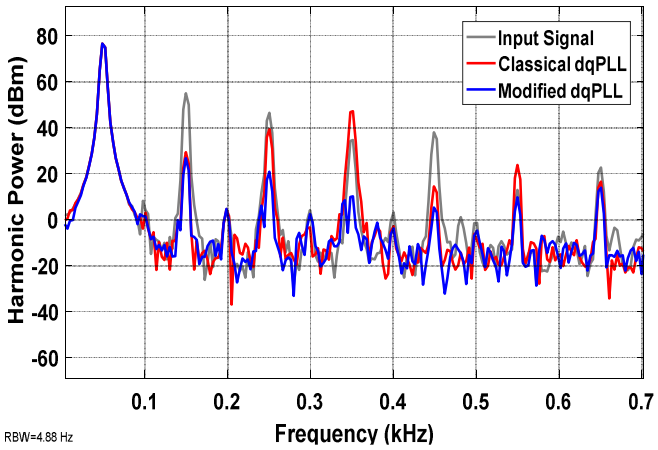

Fig. 15. Harmonic power spectrum.

TABLE II. HARMONIC POWER ANALYSIS BETWEEN THE INPUT PHASE VOLTAGE SOURCE AND THE OUTPUTS OF THE dqPLL STRUCTURES

Harmonic	Input phase voltage source power (dBc)	Output power (dBc)	
		Classical dqPLL structure	Modified dqPLL structure
1	76.52 (dBm)	76.50 (dBm)	76.49 (dBm)
2	-68.30	-73.51	-75.06
3	-21.55	-47.12	-49.82
4	-73.26	-71.91	-71.85
5	-30.02	-37.19	-55.66
6	-72.37	-79.91	-74.01
7	-41.94	-29.40	-66.37
THD (dBc)	-20.87 (9.052%)	-28.66 (3.688%)	-48.66 (0.3688%)

TABLE III. COMPARISON OF THE MODIFIED dqPLL ARCHITECTURE WITH OTHER PLL ARCHITECTURES

PLL structure	Frequency settling time (ms)	Overshoot (Hz)	Input THD value (%)	Output THD value (%)
Modified dqPLL	300	6	10.69 (5th)	0.002
ddsrfPLL [17]	55	4.08	10 (5th)	-
dαβPLL [17]	75	4	10 (5th)	-
DNαβPLL [17]	75	4	10 (5th)	-
MAFPLL [17]	300	0.7	10 (5th)	-
EPMAFPLL [17]	114	0.95	10 (5th)	-
EPMAF PLL type2 [17]	120	0.58	10 (5th)	-
SRF PLL	-	-	12.09	12.09
EPLL	-	-	12.09	0.28
QPLL	-	-	12.09	3.60
DSOGI PLL [13]	-	-	12.09	4.04

Tables III and IV compare the performance of the modified dqPLL architecture with other PLL architectures reported in the

literature in terms of settling time, overshoot, and input/output THD values. They also present a comparison between the simulation results obtained with the modified dqPLL using a generated input signal and those using a real input signal. Table III demonstrates the effectiveness of the modified dqPLL architecture in reducing the THD of the input signal. Although our improved dqPLL architecture exhibits longer settling times, they are still comparable to those of other state-of-the-art architectures. However, its main advantage is its immunity to harmonic distortion at the PLL output, as demonstrated by a reduction in harmonic distortion from 9.052% to 0.36% in the real signal study.

TABLE IV. COMPARISON OF SIMULATION RESULTS FOR THE MODIFIED DQPLL ARCHITECTURE USING A GENERATED INPUT VOLTAGE SIGNAL AND A REAL INPUT SIGNAL

PLL structure	Frequency settling time (s)	Overshoot (Hz)	Input THD value (%)	Output THD value (%)
Enhanced dqPLL (simulated signal)	0.3	6	10 (5th)	0.002
Enhanced dqPLL (simulated signal)	0.25	9	14.1 (5,7,11,13th)	0.03
Enhanced dqPLL (real signal)	0.8	9	9.052 (5,7,11,13th)	0.36

VI. CONCLUSION

The novelty proposed in this article is a new three-phase Phase-Locked Loop (PLL) architecture designed for smart grid three-phase grid-tied inverters, exhibiting superior performance in Total Harmonic Distortion (THD) reduction. The proposed design incorporates an additional tuned harmonic filtering module capable of detecting significant harmonic frequencies at various speeds. This PLL design is robust against noise and harmonic distortion.

Based on digital simulations performed in MATLAB, and offline analysis using both a MATLAB-generated signal and a real three-phase voltage vector acquired via an NI ELVIS II board (hardware) and LabVIEW (software), the proposed modified dqPLL demonstrates good steady-state and transient performance under harmonic distortion. The proposed dqPLL architecture reduces the THD from 10% to 0.36% in the real signal study, which represents a 96.4% THD reduction. Compared to other works presented in the literature, the proposed architecture exhibits the best THD reduction. However, the lock-up time of our architecture requires further optimization due to the excessive use of analog filters. Therefore, as future work, we can replace the analog filters with optimized digital filters to improve the lock-up time and proceed with digital hardware implementation and online hardware testing.

REFERENCES

[1] C. J. Melhorn, T. D. Davis, and G. E. Beam, "Voltage sags: their impact on the utility and industrial customers," *IEEE Transactions on Industry Applications*, vol. 34, no. 3, pp. 549–558, May 1998, https://doi.org/10.1109/28.673725.

[2] G. Yaleinkaya, M. H. J. Bollen, and P. A. Crossley, "Characterization of voltage sags in industrial distribution systems," *IEEE Transactions on Industry Applications*, vol. 34, no. 4, pp. 682–688, Jul. 1998, https://doi.org/10.1109/28.703958.

[3] H.-S. Kim and K.-H. Kim, "Improved Phase and Harmonic Detection Scheme using Fast Fourier Transform with Minimum Sampling Data under Distorted Grid Voltage," *The Transactions of the Korean Institute of Power Electronics*, vol. 20, no. 1, pp. 72–80, Feb. 2015, https://doi.org/10.6113/TKPE.2015.20.1.72.

[4] R. Petrella, A. Revelant, and P. Stocco, "Robust grid synchronisation in three-phase distributed power generation systems by synchronous reference frame pre-filtering," in *2009 44th International Universities Power Engineering Conference*, Glasgow, UK, 2009, pp. 1–5.

[5] R. Cardoso, R. F. de Camargo, H. Pinheiro, and H. A. Gründling, "Kalman filter based synchronisation methods," *IET Generation, Transmission & Distribution*, vol. 2, no. 4, pp. 542–555, Jul. 2008, https://doi.org/10.1049/iet-gtd:20070281.

[6] A. Timbus, M. Liserre, R. Teodorescu, and F. Blaabjerg, "Synchronization methods for three phase distributed power generation systems - An overview and evaluation," in *2005 IEEE 36th Power Electronics Specialists Conference*, Dresden, Germany, 2005, pp. 2474–2481, https://doi.org/10.1109/PESC.2005.1581980.

[7] J. Svensson, "Synchronisation methods for grid-connected voltage source converters," *IEE Proceedings - Generation, Transmission and Distribution*, vol. 148, no. 3, pp. 229–235, May 2001, https://doi.org/10.1049/ip-gtd:20010101.

[8] G. Xiaoqiang, W. Weiyang, S. Xiaofeng, and S. Guocheng, "Phase locked loop for electronically-interfaced converters in distributed utility network," in *2008 International Conference on Electrical Machines and Systems*, Wuhan, China, 2008, pp. 2346–2350.

[9] H.-S. Song and K. Nam, "Instantaneous phase-angle estimation algorithm under unbalanced voltage-sag conditions," *IEE Proceedings - Generation, Transmission and Distribution*, vol. 147, no. 6, pp. 409–415, Nov. 2000, https://doi.org/10.1049/ip-gtd:20000716.

[10] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-Phase PLLs: A Review of Recent Advances," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1894–1907, Mar. 2017, https://doi.org/10.1109/TPEL.2016.2565642.

[11] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha, "Tuning of Phase-Locked Loops for Power Converters Under Distorted Utility Conditions," *IEEE Transactions on Industry Applications*, vol. 45, no. 6, pp. 2039–2047, Nov. 2009, https://doi.org/10.1109/TIA.2009.2031790.

[12] F. Sevilmiş and H. Karaca, "Performance analysis of SRF-PLL and DDSRF-PLL algorithms for grid interactive inverters," *International Advanced Researches and Engineering Journal*, vol. 3, no. 2, pp. 116–122, Aug. 2019, https://doi.org/10.35860/iarej.412250.

[13] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-Oriented Study of Advanced Synchronous Reference Frame Phase-Locked Loops," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 765–778, Feb. 2013, https://doi.org/10.1109/TPEL.2012.2204276.

[14] M. Karimi-Ghartema, "Synchronous Reference Frame PLL," in *Enhanced Phase-Locked Loop Structures for Power and Energy Applications*, Hoboken, NJ, USA: Wiley-IEEE Press, 2014, pp. 133–145.

[15] S. F. Mekhamer, A. Y. Abdelaziz, and S. M. Ismael, "Design Practices in Harmonic Analysis Studies Applied to Industrial Electrical Power Systems," *Engineering, Technology & Applied Science Research*, vol. 3, no. 4, pp. 467–472, Aug. 2013, https://doi.org/10.48084/etasr.309.

[16] T. Demirdelen, R. I. Kayaalp, and M. Tumay, "A Modular Cascaded Multilevel Inverter Based Shunt Hybrid Active Power Filter for Selective Harmonic and Reactive Power Compensation Under Distorted/Unbalanced Grid Voltage Conditions," *Engineering, Technology & Applied Science Research*, vol. 6, no. 5, pp. 1133–1138, Oct. 2016, https://doi.org/10.48084/etasr.777.

[17] "EN 50160 Report - Power Quality Standard - Power Quality Explained." Neo Messtechnik. https://www.neo-messtechnik.com/en/power-quality-explained-chapter5-en-50160-report-standard/

[18] A. A. Nazib, D. G. Holmes, and B. P. McGrath, "Decoupled DSOGI-PLL for Improved Three Phase Grid Synchronisation," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -*

ECCE Asia), Niigata, Japan, 2018, pp. 3670–3677, https://doi.org/10.23919/IPEC.2018.8507364.

[19] P. Rodríguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant Frequency-Locked Loop for Grid Synchronization of Power Converters Under Distorted Grid Conditions," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 127–138, Jan. 2011, https://doi.org/10.1109/TIE.2010.2042420.

[20] Z. Ali, N. Christofides, L. Hadjidemetriou, and E. Kyriakides, "Design of an advanced PLL for accurate phase angle extraction under grid voltage HIHs and DC offset," *IET Power Electronics*, vol. 11, no. 6, pp. 995–1008, May 2018, https://doi.org/10.1049/iet-pel.2017.0424.

[21] Z. Ali, N. Christofides, K. Saleem, A. Polycarpou, and K. Mehran, "Performance evaluation and benchmarking of PLL algorithms for grid-connected RES applications," *IET Renewable Power Generation*, vol. 14, no. 1, pp. 52–62, Jan. 2020, https://doi.org/10.1049/iet-rpg.2019.0434.

[22] Z. Ali, N. Christofides, L. Hadjidemetriou, E. Kyriakides, Y. Yang, and F. Blaabjerg, "Three-phase phase-locked loop synchronization algorithms for grid-connected renewable energy systems: A review," *Renewable and Sustainable Energy Reviews*, vol. 90, pp. 434–452, Jul. 2018, https://doi.org/10.1016/j.rser.2018.03.086.

[23] *NI Educational Laboratory Virtual Instrumentation Suite II Series (NI ELVISTM II Series) User Manual*. Accessed: Mar. 31, 2025. [Online]. Available: https://www.ni.com/docs/en-US/bundle/374629c/resource/374629c.pdf.

[24] W. Storr. "Three Phase Transformer Connections and Basics." Basic Electronics Tutorials. https://www.electronics-tutorials.ws/transformer/three-phase-transformer.html.

[25] W. Storr. "Transformer Voltage Regulation," Basic Electronics Tutorials. https://www.electronics-tutorials.ws/transformer/voltage-regulation.html.