

Design and Control of a Three-Phase T-Type Inverter using Reverse-Blocking IGBTs

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Abstract-This paper proposes the design and implementation of a 15kW three-phase T-type inverter. Fuji Electric's new generation IGBT module (V series) using RB-IGBT technology is applied for the converter, due to its higher efficiency from conventional IGBTs to reduce switching losses on the semiconductors. Under full load conditions, the overall efficiency of the converter can reach over 98%. The control design and sine PWM modulation are implemented on a DSP kit named TMS320F3F28379D. In addition, the PWM is generated with the fundamental and third harmonics of a sin wave, allowing a modulation factor up to 1,154 compared to traditional PWM. The output voltage of 220V/50Hz with less than 2% of THD can be achieved at the minimum input DC voltage of 550V.

Keywords-three-phase T-type inverter; Pulse Width Modulation (PWM); digital signal processor

I. INTRODUCTION

Nowadays, multilevel inverter structures have been researched widely because of advantages such as their modular structure, simple connection, and maintenance ease. Multi-level inverter structures have various prototypes: Neutral Point Clamped (NPC) [1], Cascaded H-Bridge (CHB) [2], Modular Multilevel Converter (MMC), and T-type inverter [3-4]. Among multilevel inverters, the T-type inverter is considered as an advance prototype of the NP converter. The output voltage of the T-type multilevel inverter reduces harmonics. Furthermore, the dimension of the reactive filter components and the amount of switching devices of the T-type inverter are reduced significantly, which improves the overall efficiency of the system. The T-type inverter is most popular in rooftop solar systems when used for the three-phase grid at the power range of 15kW [5].

Conventional IGBTs can operate at maximum switching frequency of about 20kHz and the power losses are very high. To deal with this problem, the RB-IGBT technology is used in this research to reduce power losses [6-7]. Fuji's IGBT switches are produced for integrating with T-type structure which makes operation more reliable and efficient [8]. The Pulse Width Modulation (PWM) algorithm combines fundamental and third harmonics, which improve the voltage utilization [9], and allow the converter to operate reliably at a

grid with 380V/50Hz voltage. This paper presents the design of the PWM method along with a voltage-current control, which is embedded on a TMS320F3F28379D DSP kit. The experimental system for the three-phase T-type inverter uses the RB-IGBT technology semiconductor. The experiment results verify the effectiveness of the proposed method in improving the system's efficiency.

II. THE THREE-PHASE T-TYPE INVERTER STRUCTURE USING RB-IGBT

Figure 1 presents a three-phase three-level T-type inverter structure, which consists of the conventional two-level topology with six switches ($S_{A1}, S_{A4}, S_{B1}, S_{B4}, S_{C1}, S_{C4}$), while each leg is connected to the neutral point P of a DC bus through three bidirectional switches ($S_{A2}, S_{A3}, S_{B2}, S_{B3}, S_{C2}, S_{C3}$). This circuit diagram can generate 3 levels of phase voltage (as shown in Table I) and 5 levels of line voltage: $+V_{DC}, +0.5V_{DC}, 0, -0.5V_{DC}, -V_{DC}$.

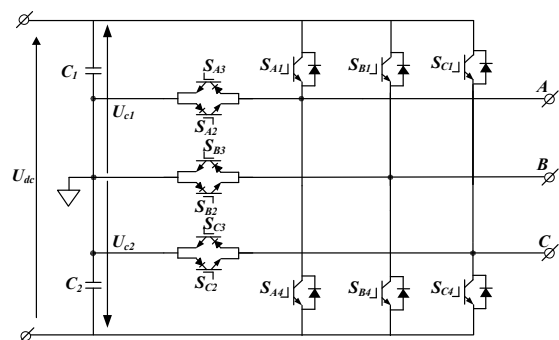


Fig. 1. Three-phase T-type inverter structure.

TABLE I. SWITCH STATUS CORRESPONDING TO VOLTAGE LEVELS AND CAPACITOR STATES

Switching state	Valve state (x = A, B, C)				Output voltage
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	
$+1/2V_{DC}$	On	Off	Off	Off	Off
0	On	Off	Off	Off	On
$-1/2V_{DC}$	Off	On	On	Off	On

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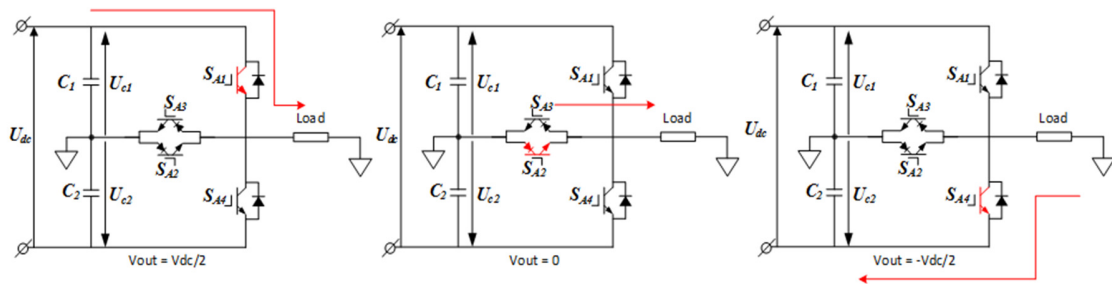


Fig. 2. Phase A current and output voltage status of the three-phase T-type inverter.

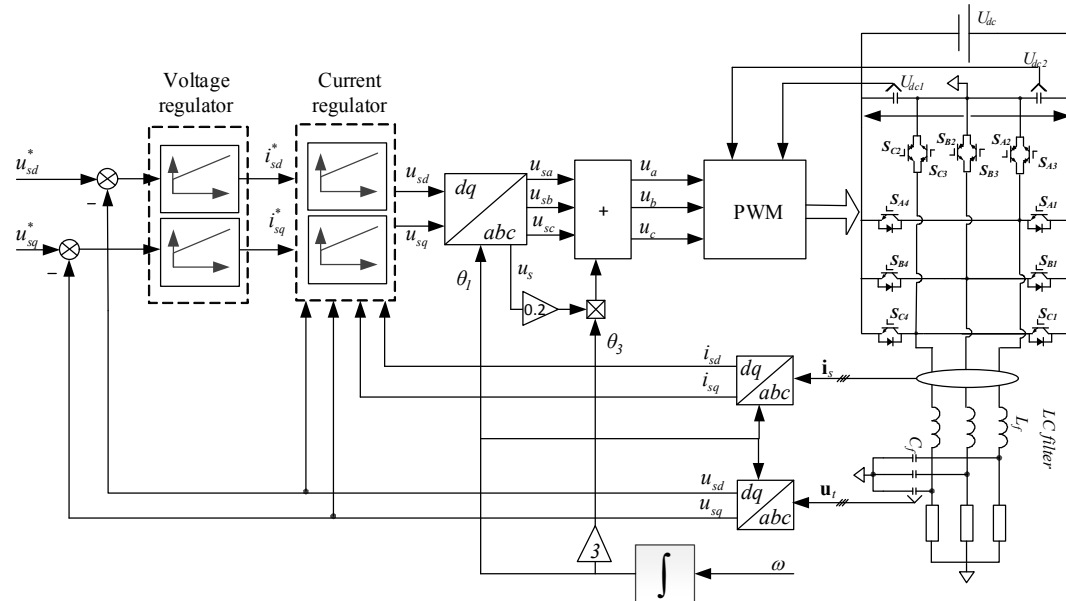


Fig. 3. The control structure of the three-phase T-type inverter applied in standalone mode.

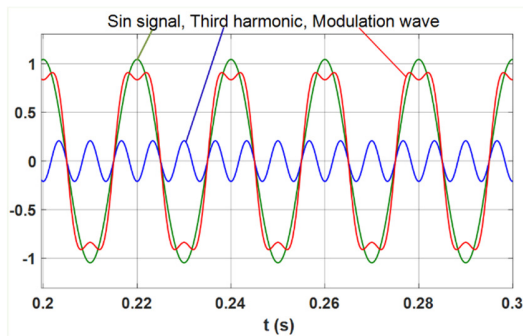


Fig. 4. Modulation method with 3rd harmonic combination.

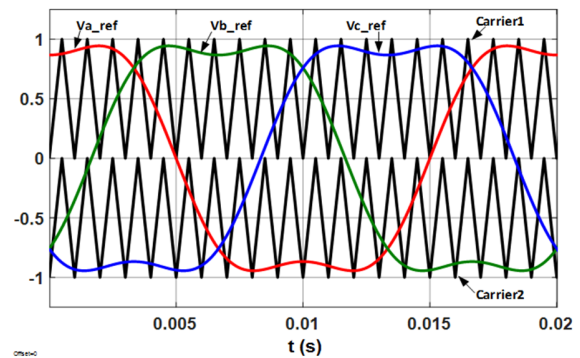


Fig. 5. The three-phase modulation index.

The operation states of the switching devices in Table I are shown in detail in Figure 2. As can be observed, only one device has switched with corresponding current path in one state. Figure 3 shows the control strategy of the three-phase T-type inverter in standalone mode. In this research, the modulation waves of each phase include single-phase standard sine wave combined with a third harmonic [10-13], as presented in Figure 4. The final modulation waves for the three phases are compared to the shift-level carrier pulse in Figure 5. Besides, by reversing the status of S_{A1} , S_{A2} , S_{B1} , S_{B2} , S_{C1} , S_{C2} ,

operate states of switches S_{A3} , S_{A4} , S_{B3} , S_{B4} , S_{C3} , S_{C4} can be obtained, respectively. In the three-phase system, the voltage vector u_s is represented by u_a , u_b , u_c with 120° phase angles between them:

$$u_a = m_a \cos(\omega t) \quad (1)$$

$$u_b = m_a \cos\left(\omega t - \frac{2}{3}\pi\right) \quad (2)$$

$$u_c = m_a \cos\left(\omega t + \frac{2}{3}\pi\right) \quad (3)$$

where m_a is duty cycle of the PWM modulation method (Figure 4). According to [14], the third harmonic injected u_0 (THI) is added to the fundamental sine wave with amplitude equal to 0.2 times that of the voltage amplitude u_s :

$$V_{a_ref} = u_a + u_0 \quad (4)$$

$$V_{b_ref} = u_a + u_0 \quad (5)$$

$$V_{c_ref} = u_a + u_0 \quad (6)$$

where:

$$u_o = 0.2m_{a_max} \cos(3\omega t) = 0.2 \cos(3\omega t) \quad (7)$$

Equations (8)-(9) illustrate the linear relationship between the output current and the control signal is the corresponding voltage:

$$\begin{cases} v_{sd}^* = rL i_{sd} + L_f \frac{di_{sd}}{dt} - \omega_s L_f i_{sq} + v_{Ld} \\ v_{sq}^* = rL i_{sq} + L_f \frac{di_{sq}}{dt} - \omega_s L_f i_{sd} + v_{Lq} \end{cases} \quad (8)$$

$$\begin{cases} v_{sd}^* = \Delta v_d + v_{Ld} - \omega_s L_f i_{sq} \\ v_{sq}^* = \Delta v_q + v_{Lq} - \omega_s L_f i_{sd} \end{cases} \quad (9)$$

The cross-channeled components and the noise of load voltage are removed by cross-compensation and the integral part of the current controller, as shown in Figures 6-7.

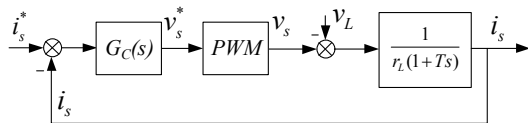


Fig. 6. The current loop structure.

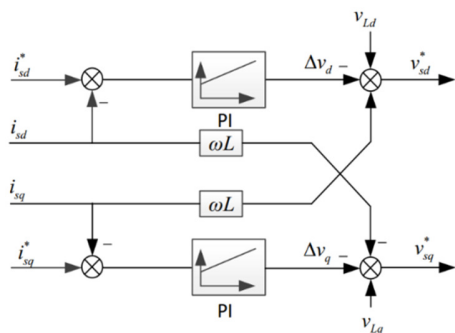


Fig. 7. The decoupling current control for the three-phase T-type inverter.

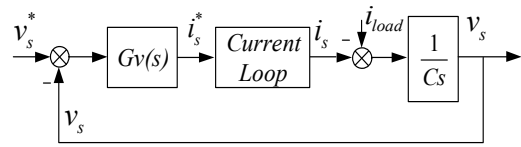


Fig. 8. The voltage loop structure

The mathematical model of the voltage controller is similar to the current controller's in dq coordinates. The three-phase currents based on Kirchoff equation are transformed into rotary d-q coordinates with fundamental rotating speed of output voltage ω :

$$\begin{cases} i_{sd} = i_{Ld} + C_f \frac{dv_{Ld}}{dt} - \omega_s L_f i_{sq} \\ i_{sq} = i_{Lq} + C_f \frac{dv_{Lq}}{dt} - \omega_s C_f i_{sd} v_{Ld} \end{cases} \quad (10)$$

Assuming that the close-loop of the transfer current is approximately 1, the relationship between load and reference voltage is rewritten from (9):

$$\begin{cases} \frac{v_{Ld}(s)}{i_{sd}^*(s)} \approx \frac{1}{C_s} \\ \frac{v_{Lq}(s)}{i_{sq}^*(s)} \approx \frac{1}{C_s} \end{cases} \quad (11)$$

By applying Clarke and Park transforms, the control method in this paper implements the PI controller for current components in d-q coordinates. The current controller uses the cross-channeled control which is based on the control method of three-phase AC machines [15]. The outputs of the current controller are converted to abc coordinates by Park transform, then they are added to THI to obtain the duty cycle. Finally, the duty cycle will be applied in the PWM modulator to generate the pulses for the switching devices.

III. PROTOTYPE IMPLEMENTATION

The DSP TMS320F28379D is a static 32bit microcontroller of Texas Instruments. The microcontroller series allows operation with quartz frequencies up to 200MHz. In addition, it integrates the 32-bit floating-point arithmetic engine called CLA (Control Law Accelerator) for computational processing. The control algorithm is run in parallel with the other tasks on the CPU. The control structure for the T-type multi-level converter is implemented on the DSP. The time frame of the program on DSP for the converter is shown on Figure 9. PWM1 is initialized in "up-down" mode, generating pulses at 10kHz, and after 2 periods, the ADC is triggered when the counter of PWM equals to TBPRB. The ADC A0, A1, A2, B2, C2, A3, B3, C3 start converting the analog signals (u_{dc1} , u_{dc2} , u_{sa} , u_{sb} , u_{sc} , i_{sa} , i_{sb} , i_{sc}). When the ADC conversion is done, the program in CLA interrupt is triggered (task1). The current controller is executed with the 200us-sampling-period T_i , which is twice the pulse period T_{pulse} . The output voltage controller is executed with the 2ms-sampling-period, which is

ten times the sampling period of the current controller. After finishing the calculation in CLA, the new duty cycle values are updated to PWM registers. Before updating the value to the PWM channels for the next time, the calculation of the modulation index must be conducted. The PWM value is updated at the instant when the counter of the PWM channel equals to 0. So, the execution time of the program must be less than the half of the period cycle, which is about 50μs. As can be observed, the total program execution time of only 4.89μs is smaller than this time limitation. The experimental system uses a three-phase bridge rectifier and capacitor system to generate DC voltage. To increase the DC voltage, a 24.7kW transformer is applied in front of the rectifier bridge along with a capacitor system to reduce DC voltage fluctuations on the DC bus. The three-phase T-type inverter system is controlled in a stand-alone mode. A Yokogawa M&C Corporation CW140 [16] Clamp-on Power Meter is connected to measure the input and output of the converter to evaluate the efficiency as shown on Figure 10.

TABLE II. REAL CIRCUIT PARAMETERS

Sign	Parameters	Value
V_{DC}	Input DC voltage	600VDC
V_{rms}	Output phase voltage	220VAC
f_i	Basic frequency	50Hz
f_s	Pulse frequency	10kHz
L_f	Filter inductors	0.8mH
r_f	Inductors resistor	0.1Ω
C_f	Filter capacitors	20μF
C_1, C_2	DC capacitors	940μF
IGBT Fuji	12MBI100VN-120-50 (1.2kV/100A)	
Controller Card	TMS320F28379D	

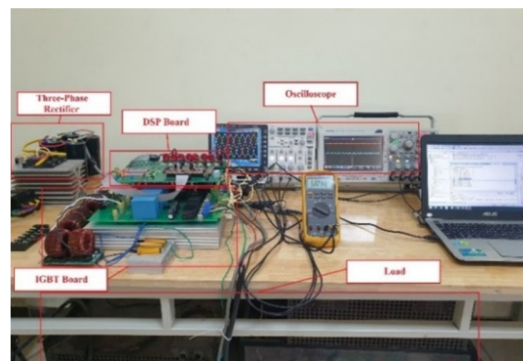


Fig. 11. The experimental model of the three-phase T-type inverter.

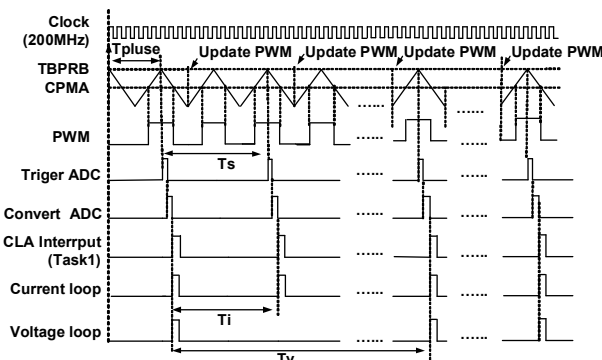


Fig. 9. Time frame of implementation on the DSP.

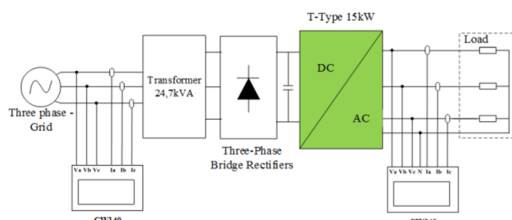


Fig. 10. The experimental model of the three-phase T-type inverter.

IV. EXPERIMENTAL RESULTS

The experiment parameters of the control system are shown in Table II. The modulation of the third harmonic is shown on Figure 12. Figure 13 illustrates u_{sd} and u_{sq} voltage responses. Figure 14 shows i_{sd} and i_{sq} current responses on d-q coordinates, which are moved out to DAC of the control card. Similarly, voltages u_{sd} and u_{sq} are set to be $220\sqrt{2}$ and 0 respectively, so that the power factor equals to 1. The output of the voltage controller is the set value for the current controller. The set value of the voltage controller ramps in 0.5s time. This ramp could reduce and prevent the system from over-current and over-voltage while starting. Besides, the responses of the controllers are not affected while changing loads.

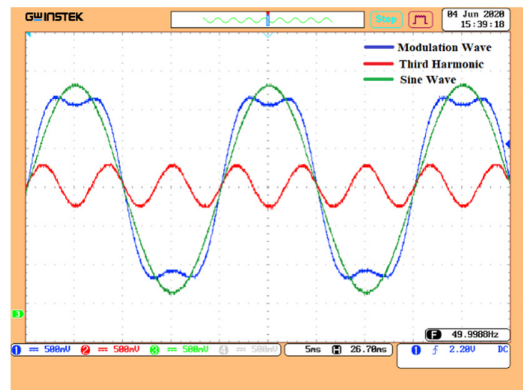


Fig. 12. Modulation method with 3rd harmonic combination.

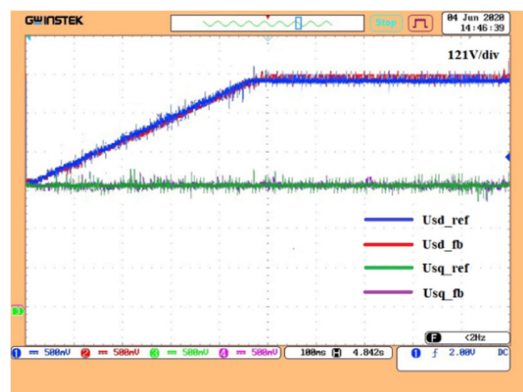


Fig. 13. u_{sd} and u_{sq} voltage responses.

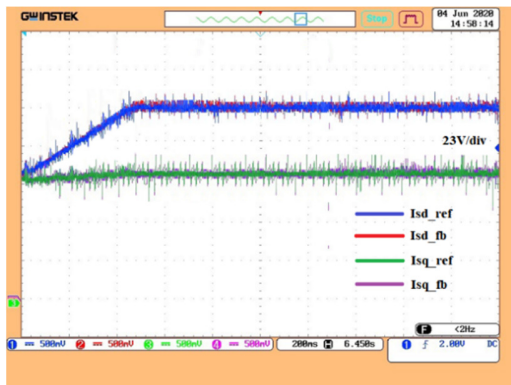


Fig. 14. I_{sd} and I_{sq} current responses.

The voltage of the DC bus is 560V as shown in Figure 15, and the voltages on C_1 and C_2 capacitors fluctuate around 280V. Figure 16 illustrates the fluctuation of voltages on C_1 and C_2 , with the magnitude $\Delta V_C=10V$. The voltage of the DC bus is fluctuating due to the diode bridge rectifier. Three-phase load current, output line voltage Vab before filter, and LC filter output three-phase voltage are shown in Figures 18, 19, and 20 respectively. The output voltage of the three-phase T-type inverter has an rms value of 220V and the THD is 2.7%, at 15kW. The efficiency reaches its highest value of over 98%, as presented in Figure 17 under full-load condition. Since the input DC power is powered by a 3-phase diode rectifier, the DC voltage ripples 6 times to grid voltage frequency.

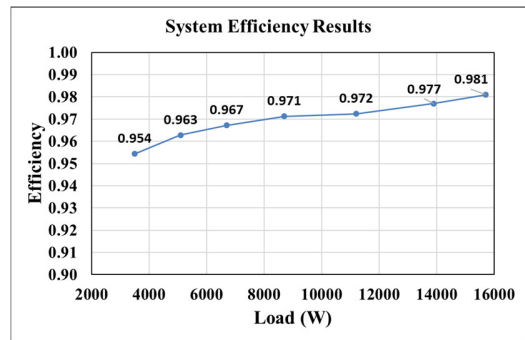


Fig. 17. The converter's efficiency.

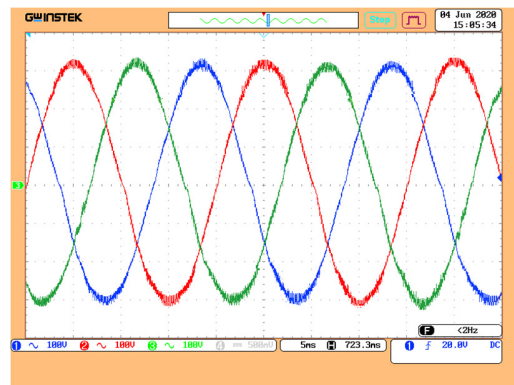


Fig. 18. The three-phase load currents.

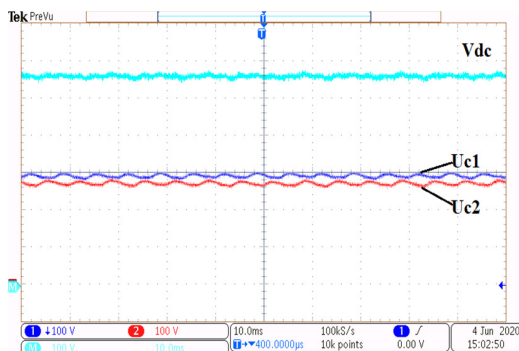


Fig. 15. The voltages on C_1 and C_2 capacitors and the DC bus voltage.

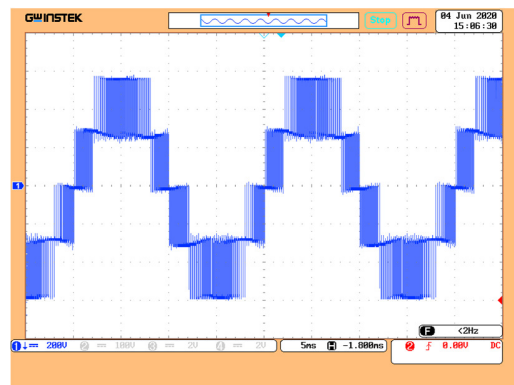


Fig. 19. Output line voltage before filter.

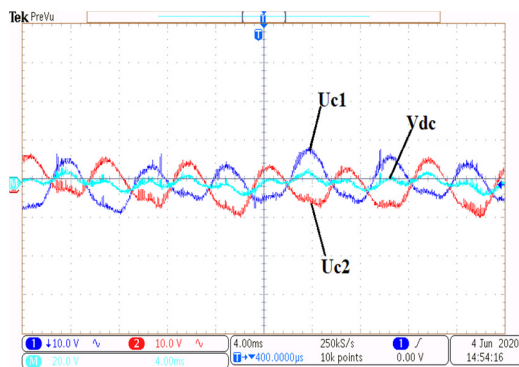


Fig. 16. The difference of voltages between capacitors.

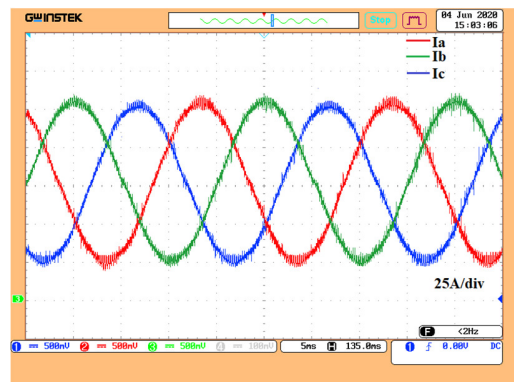


Fig. 20. The LC filter output phase voltages.

V. CONCLUSION

In the current paper, a three-phase T-type inverter at the power range of 15kW was designed and implemented. The controller card TMS320F28379D which is capable of calculating floating-point and processing signals quickly was utilized in this research. The PWM-THI modulation method is applied due to its higher than conventional PWM modulation factor. After combining the modulation and control methods, the stand-alone three-phase T-type inverter with input voltage of 600V is controlled stably to generate an output voltage of 220V, with power rating of 15kW with 2.7% current THD and 98% full-load condition efficiency.

REFERENCES

- [1] M. Rezki and I. Griche, "Simulation and Modeling of a Five -Level (NPC) Inverter Fed by a Photovoltaic Generator and Integrated in a Hybrid Wind-PV Power System," *Engineering, Technology & Applied Science Research*, vol. 7, no. 4, pp. 1759–1764, Aug. 2017, <https://doi.org/10.48084/etasr.1271>.
- [2] Y. Gopal, K. P. Panda, D. Birla, and M. Lalwani, "Swarm Optimization-Based Modified Selective Harmonic Elimination PWM Technique Application in Symmetrical H-Bridge Type Multilevel Inverters," *Engineering, Technology & Applied Science Research*, vol. 9, no. 1, pp. 3836–3845, Feb. 2019, <https://doi.org/10.48084/etasr.2397>.
- [3] R. A. Rana, S. A. Patel, A. Muthusamy, C. woo Lee, and H.-J. Kim, "Review of Multilevel Voltage Source Inverter Topologies and Analysis of Harmonics Distortions in FC-MLI," *Electronics*, vol. 8, no. 11, Nov. 2019, Art. no. 1329, <https://doi.org/10.3390/electronics8111329>.
- [4] C. L. Solanki, M. H. Ayalani, and S. N. Gohil, "Performance of Three Phase T-Type Multilevel Inverter with Reduced Switch Count," in *2018 International Conference on Current Trends towards Converging Technologies (ICCTCT)*, Mar. 2018, pp. 1–5, <https://doi.org/10.1109/ICCTCT.2018.8550937>.
- [5] A. Salem and M. A. Abido, "T-Type Multilevel Converter Topologies: A Comprehensive Review," *Arabian Journal for Science and Engineering*, vol. 44, no. 3, pp. 1713–1735, Mar. 2019, <https://doi.org/10.1007/s13369-018-3506-6>.
- [6] C. Klumpner and F. Blaabjerg, "Using reverse-blocking IGBTs in power converters for adjustable-speed drives," *IEEE Transactions on Industry Applications*, vol. 42, no. 3, pp. 807–816, May 2006, <https://doi.org/10.1109/TIA.2006.872956>.
- [7] T. Naito, M. Takei, M. Nemoto, T. Hayashi, and K. Ueno, "1200V reverse blocking IGBT with low loss for matrix converter," in *2004 Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs*, Kitakyushu, Japan, May 2004, pp. 125–128, <https://doi.org/10.1109/WCT.2004.239842>.
- [8] P. J. Grbovic, F. Gruson, N. Idir, and P. L. Moigne, "Turn-on Performance of Reverse Blocking IGBT (RB IGBT) and Optimization Using Advanced Gate Driver," *IEEE Transactions on Power Electronics*, vol. 25, no. 4, pp. 970–980, Apr. 2010, <https://doi.org/10.1109/TPEL.2009.2031805>.
- [9] M. Sajitha, J. Sandeep, and R. Ramchand, "Comparative Analysis of Different Modulation Techniques for Three Level Three Phase T-type NPC Inverter," in *TENCON 2019 - 2019 IEEE Region 10 Conference (TENCON)*, Kochi, India, Oct. 2019, pp. 1529–1534, <https://doi.org/10.1109/TENCON.2019.8929574>.
- [10] J. Huang, Q. Liu, X. Wang, and K. Li, "A Carrier-Based Modulation Scheme to Reduce the Third Harmonic Component of Common-Mode Voltage in a Three-Phase Inverter Under High DC Voltage Utilization," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 1931–1940, Mar. 2018, <https://doi.org/10.1109/TIE.2017.2745439>.
- [11] A. Yang, L. Pamungkas, Y. Chang, J. Lin, and H. Chiu, "Design and Implementation of 6 kW Three-Phase T-Type Inverter for Microgrid Application," in *2018 International Conference on Applied Engineering (ICAE)*, Batam, Indonesia, Oct. 2018, pp. 1–5, <https://doi.org/10.1109/INCAE.2018.8579417>.
- [12] J. Jose, G. N. Goyal, and M. V. Aware, "Improved inverter utilisation using third harmonic injection," in *2010 Joint International Conference on Power Electronics, Drives and Energy Systems 2010 Power India*, Dec. 2010, pp. 1–6, <https://doi.org/10.1109/PEDES.2010.5712490>.
- [13] L. Chaturvedi, D. K. Yadav, and G. Pancholi, "Comparison of SPWM, THIPWM and PDPWM Technique Based Voltage Source Inverters for Application in Renewable Energy," *Journal of Green Engineering*, vol. 7, no. 1, pp. 83–98, Jan. 2017, <https://doi.org/10.13052/jge1904-4720.7125>.
- [14] W. Subsingha, "A Comparative Study of Sinusoidal PWM and Third Harmonic Injected PWM Reference Signal on Five Level Diode Clamp Inverter," *Energy Procedia*, vol. 89, pp. 137–148, Jun. 2016, <https://doi.org/10.1016/j.egypro.2016.05.020>.
- [15] N. Dong, H. Yang, J. Han, and R. Zhao, "Modeling and Parameter Design of Voltage-Controlled Inverters Based on Discrete Control," *Energies*, vol. 11, no. 8, Aug. 2018, Art. no. 2154, <https://doi.org/10.3390/en11082154>.
- [16] M. Kawasaki, K. Funaki, and A. Morita, "CW140 Clamp-on Power Meter," Yokogawa Technical Report English Edition 31, 2001.